Elmo Luiz Fechine Sette

Layout-Oriented Design of a 60 GHz Power Amplifier in SiGe Technology

João Pessoa, Brasil

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PROF. DR. ANTONIO AUGUSTO LISBOA DE SOUZA (Presidente)

PROF. DR. EMMANUEL BENOIT JEAN-BAPTISTE DUPOUY

PROF. DR. WASLON TERLLIZZIE ARAÚJO LOPES

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Abstract

This work presents the design of a fully integrated cascode single-stage power amplifier for 60 GHz band. The technology used in the design was Global Foundries SiGe of 0.13μm (BiCMOS8HP). A load-pull analysis of the cascode was done including optimization of the bias and geometry parameters aiming at finding the best performance of this topology. A layout-oriented design approach was adopted to decide upon different combinations/arrangements of passive components and interconnections, aiming at reducing the global losses and, thus, increasing the energy efficiency of the amplifier. Post-layout simulations show a saturated output power of 19.32 dBm, 27.8% of power added efficiency (PAE) and a power gain of 10.4 dB at 60 GHz. The amplifier consumes 63 mA from a 4.4 V power supply and occupies an area of approximately 0,475 mm^2. The circuit was taped-out in late 2017. Experimental results are presented at the end of the text.

Keywords: Cascode, Layout-oriented, Load-Pull, Millimeter Wave, Power Amplifier, SiGe, 60 GHz.

Resumo

Este trabalho apresenta o projeto de um amplificador de potência totalmente integrado de estágio único e com topologia *cascode* para a banda de 60 GHz. Foi utilizada no projeto a tecnologia da Global Foundries em SiGe de 0,13 μm (BiCMOS8HP). Uma análise *load-pull* do *cascode* foi feita incluindo otimização dos parâmetros de polarização e geometria visando encontrar o melhor desempenho possível desta topologia. Uma abordagem de projeto orientado a *layout* foi adotada para decidir entre diferentes combinações/arranjos de componentes passivos e interconexões, visando reduzir as perdas globais e, portanto, aumentar a eficiência energética do amplificador. Simulações pós-*layout* demonstram uma potência de saída saturada de 19,32 dBm, 27,8 % de PAE e um ganho de potência de 10,4 dB em 60 GHz. O amplificador consome 63 mA de uma fonte de alimentação de 4,4 V e ocupa uma área de aproximadamente 0,475 mm^2. O circuito foi enviado para fabricação no final de 2017. Os resultados experimentais são apresentados ao final do texto.

Palavras-chave: Amplificador de Potência, Cascode, *Load-Pull*, Ondas Milimétricas, Orientado a *Layout*, SiGe, 60 GHz.

Resumen

Este proyecto presenta el diseño de un amplificador de potencia cascode de etapa única completamente integrado para la banda de 60 GHz. La tecnología utilizada en el diseño fue Global Foundries SiGe de 0,13 μm (BiCMOS8HP). Se realizó un análisis de *load-pull* del cascode que incluyó la optimización de los parámetros de polarización y geometría con el objetivo de encontrar el mejor rendimiento posible de esta topología. Se adoptó un enfoque de diseño orientado a *layout* para decidir sobre diferentes combinaciones/arreglos de componentes pasivos e interconexiones, con el objetivo de reducir las pérdidas globales y así aumentar la eficiencia energética del amplificador. Las simulaciones posteriores al *layout* demuestran una potencia de salida saturada de 19,32 dBm, 27,8% de PAE y una ganancia de potencia de 10,4 dB a 60 GHz. El amplificador consume 63 mA de una fuente de alimentación de 4,4 V y ocupa un área de aproximadamente 0,475 mm^2. El circuito fue enviado a la fabricación a finales de 2017. Los resultados experimentales se presentan al final del texto.

Palabras clave: Amplificador de Potencia, Cascode, *Load-Pull*, Ondas Milimétricas, Orientado a *Layout*, SiGe, 60 GHz.

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List of abbreviations and acronyms

4G	Fourth generation of mobile systems
5G	Fifth generation of mobile systems
ACLR	Adjacent Channel Leakage Ratio
ADS	Advanced Design System
AM-AM	Amplitude-Amplitude Conversion
AM-PM	Amplitude-Phase Conversion
AR/VR	Augmented Reality/Virtual Reality
BEOL	Back-End-of-Line
BJT	Bipolar Junction Transistors
BiCMOS	Bipolar-CMOS
CB	Common-Base
CE	Common-Emitter
CAD	Computer Aided Design
DAT	Distributed Active Transformers
DRC	Design Rules Check
DUT	Device Under Test
ECMA	European Computer Manufacturers Association
EVM	Error Vector Magnitude
FOM	Figure of Merit
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GF	Global Foundries
GSG	Ground-Signal-Ground
HBT	Heterojunction Bipolar Transistors
HEMT	High Electron Mobility Transistors
IFPB	Federal Institute of Paraíba
InP	Indium Phosphide

ITU	International Telecommunication Union
LNA	Low Noise Amplifier
LO	Local Oscillator
LSSP	Large Signal S-Parameters
MIM	Metal Insulator Metal
mmW	millimeter Wave
NF	Noise Figure
OFDM	Orthogonal Frequency Division Multiplexing
PA	Power Amplifier
PAE	Power Added Efficiency
PHY	Physical Layer
PVT	Process, Voltage and Temperature
PZ	Poles and Zeros
RF	Radio Frequency
R&D	Research and Development
SC	Single Carrier
SiGe	Silicon-Germanium
SiO2	Silicon Dioxide
T-lines	Transmission lines
UFPB	Federal University of Paraíba
VNI	Visual Network Index
VNA	Vector Network Analyzer
WRC	World Radiocommunication Conference
WiGig	Wireless Gigabit Alliance
WLAN	Wireless Local Area Network
WPAN	Wireless Personal Area Network
WVAN	Wireless Video Area Network

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Introduction

In the last few years wireless communication industry had enormous growth due to the increasing demand of wireless devices. Nowadays, millions of people around the world are daily online exchanging data to each other through their smartphones, tablets and laptops. This huge demand for services are saturating the spectrum below 6 GHz, where mobile and data communication (3G, 4G) are usually done. This spectrum will no longer be sufficient to meet the ever-growing demand of consumers, who want all their devices to be online been able to record, transfer and monitor a large amount of data with increasing data rates.

The demand for content will continue to grow at extreme rates, which can be seen thanks to the annual Visual Network Index (VNI) released by Cisco (CISCO, 2017). The most recent (September 2017) report shows a demand of 278 Exabyte per month by 2021, representing an increasing of almost 100 times since 2010. In addition to the large amount of data, the number of devices and data rates will continue to grow exponentially (ANDREWS et al., 2014).

While the memory capacity and clock speed of computers have increased by a few orders of magnitude in recent decades, the frequency of wireless carriers ranged from just 0.8 to 5.8 GHz (RAPPAPORT et al., 2011). This limited spectrum allows data rate of only a few hundred Mb/s in the fourth generation (4G), mainly due to spectral congestion that heavily limits its bandwidth.

The necessity of a high rate and volume of data makes inevitable the migration of the carriers to beyond the Radio Frequency (RF) band, due to this one be relatively small compared to the vast free spectrum between 6 and 300 GHz (RAPPAPORT et al., 2015), fomenting the bases of what will become the fifth generation of mobile communication (5G). In this way, millimeter wave circuits (mmW) became a hot topic of this last decade, representing the most challenging and exciting opportunities for electronic engineers in the field of circuits design, antennas and communications systems (RAPPAPORT et al., 2011). Inside the millimeter wave band, there is a frequency range around 60 GHz that attracts more interest. The unlicensed band between 57 and 64/66 GHz becomes one of the most attractive option for the next generation mobile system (5G), for allowing an extremely high data rate (within the Gb/s range), and availability of a large free frequency band without any neighboring standards. The oxygen absorption at this band allows high attenuation of the signals that cross the environment, making these ideal for densely pack electronic media for short-range communication (RAPPAPORT et al., 2011).

At such high frequencies the design of transceivers becomes challenging, since any parasitic element can significantly impact the behavior of the circuit. On the other hand, working at such high frequencies brings one advantage. In 60 GHz, the wavelength of approximately 2.5 millimeter in silicon dioxide (SiO_2), allows a high density of integration of analog and microwave components, such as transmission lines and antennas, allowing the implementation of fully integrated topologies that were not possible at lower frequencies.

One of the main blocks in a transmitter is the power amplifier (PA), being the one in charge to amplifying the signal to such levels that can be radiated by the antenna. Thus, this block is the main responsible for the power consumption in a transmitter system. Its main performance characteristics are the power delivered to the load, power added efficiency (PAE), power gain and linearity.

In the last decade, the design of PAs in the millimeter wave range was performed in technologies based on semiconductors of group III-V[1]. These technologies were preferred for allowing a high frequency of operation when compared to the technologies based on silicon of that time. On the other hand, such manufacturing processes are relatively expensive, and do not allow easy integration with the digital part of the circuit. The continued process scaling in SiGe technology allowed the heterojunction bipolar transistor (HBT) to become sufficiently fast for operations in millimeter waves. These achieved a transition frequency of 505 GHz and a maximum oscillation frequency of up to 720 GHz (IHP, 2016), making it the main competitor of group III-V semiconductors in terms of high frequency performance. The drawback of this process is the reduction of breakdown voltages, making difficult to achieve large output power. Therefore the power amplifier is one of the most challenging blocks to be designed at this band.

The goal of this work was the investigation, analysis and design of power amplifiers in the band of millimetric waves, having the 60 GHz frequency as central. The great challenge of designing circuits in this frequency range is the impact caused by all the parasitic elements that arise as a result of the design of the layout. These parasitics arise from the several metal layers used to interconnect the components (passive and active), and which do not present a model in the schematic. At such high frequencies any parasitic elements, however small (e.g. fF capacitances or mΩ resistances), can significantly impact the behavior of the amplifier by introducing losses and mismatches. For this reason the classical design approach, in which the circuit is completely designed in the schematic level to then be designed the entire layout, may not yield satisfactory results, that is, there can be a huge discrepancy between the results of the schematic and the layout. Due to this difficulty in reaching a good relation between schematic and layout results in very high frequencies, a layout-oriented design approach was proposed. This was adopted to decide upon different combination/arrangements of passive components and interconnections,

[1] The group III-V are the semiconductors made up of elements from group III and V of the periodic table, such as GaAs, GaN, InP.

aiming at reducing the global losses of the PA, thus increasing its efficiency. This approach was divided in steps, where each one is optimized by successive layout iteractions (iterative method) in order to establish the best relation between schematic and layout results, thus providing the expected performance.

This master's thesis took place in the RFWild laboratory located at the Federal University of Paraíba (UFPB) and Federal Institute of Paraíba (IFPB) in Brazil. The research group was established in 2013. This group develops researches in the area of microelectronics (design and modeling), instrumentation and Research and Development (R&D). The laboratory has undergraduates and masters students working on these projects. Further information about the laboratory and the projects developed by this group can be find at (RFWILD, 2018).

This work was carried out using all the infrastructure and the Computer Aided Design (CAD) tools of the RFWild's laboratory, and through the use of the Global Foundries (GF) SiGe BiCMOS8HP technology process of 0.13 μm.

The rest of the document is organized as follows: Chapter 1 brings a literature review of the main fundamentals for a good understanding of the design procedure of this work. In Chapter 2 we describe the components of the technology used and their characteristics. In Chapter 3 we describe the design procedure methodology while Chapter 4 presents and discusses the results obtained. Finally, Chapter 5 draws the conclusions and discusses the prospects of this work.

1 Literature Review

1.1 A brief overview of power amplifiers

The transceiver is the element responsible for RF signal modulation/demodulation, enabling wireless communication through high frequency signals. This is made up of two stages, one responsible for the transmission (transmitter) and the other responsible for the reception (receiver) of the signal. The performance of these blocks depends directly on the individual performance of each circuit that constitutes it, and of the set as a whole. In communication systems these transceivers can be implemented in different architectures. A typical architecture of an RF transceiver is shown in Figure 1.

After the information is converted to the baseband, the signal is processed digitally. The trend is that the digital processing is getting closer and closer to the antenna, thus reducing costs and increasing system flexibility (LEE, 2004). Afterward digital processing, the signal is suited in order to be able to be transmitted in the environment. In the receiver stage the design of the following RF circuits stand out: Low Noise Amplifier (LNA), local oscillators (LO) and mixer. In the transmitter the LNA is replaced by a power amplifier (PA). Its design is of great interest for the transmitter chain, since it may represent the majority part of the consumption of an entire transceiver. A simplified power amplifier features three main stages as shown in Figure 2. It is composed of an input matching network, an amplifier stage and an output matching network, besides the bias circuitry. Power amplifiers should provide a high output power with the best possible efficiency, in order to increase the autonomy of battery-powered systems. Besides these ones, the design of a PA requires take in account other parameters that characterize the good performance of the circuit. In this way the RF design engineer must be able to establish the best trade-off between output power, efficiency, gain, linearity, among others,

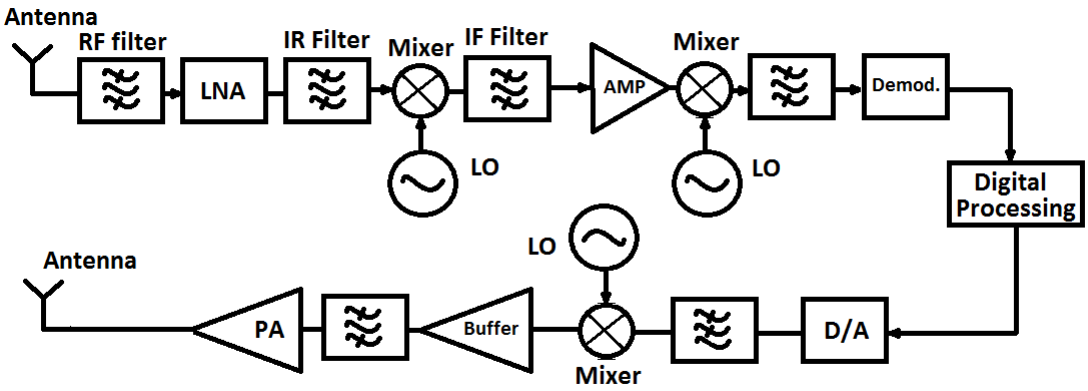

Figure 1 – Typical architecture of a transceiver.

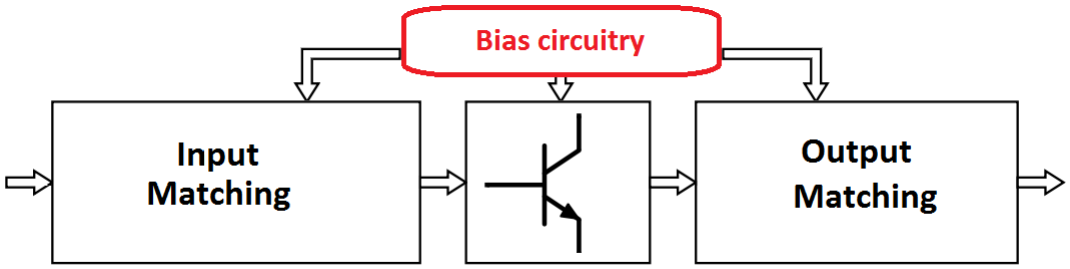

Figure 2 – Simplified diagram of a power amplifier.

for a given situation. These are used as performance parameters of the circuit and allow comparison with the state of the art. The next subsection will introduce some of the key performance characteristics of power amplifiers.

1.1.1 Key performance parameters

1.1.1.1 Output power and saturated output power

One of the main goals in designing a PA is to deliver a certain power to a load. Output power is one of the main performance characteristics of the amplifier, being its maximum value determined largely by the load impedance and the power supply (ROGERS; PLETT, 2010). The theoretical maximum power (at fundamental frequency) in a purely resistive load would be defined by:

$$P_{out} = \frac{V_{out}^2}{2R_L} \tag{1.1}$$

where V_{out} is the peak output voltage in the frequency of interest and R_L is the load (generally 50Ω). The diagram in Figure 3 shows the power balance in a PA. The output power (P_{out}) is defined as the one delivered to the load to which the amplifier is connected. P_{in} represents the power effectively entering in the amplifier, while P_{disp} is the power available at the output of this. P_{avs} represents the power available from the source, while P_{dc} is the DC power dissipated at the amplifier. The characteristic source and load impedances (Z_S e Z_L) are generally equal to 50 Ω. In Figure 4 the relation between the output power (P_{out}) and the power available by the source (P_{avs}) for an implemented generic power amplifier is shown. In this graph, the evolution of the output power is observed as a function of the increasing available input power. The highest possible value that P_{out} can achieve is called saturated output power (P_{sat}). In this region increments in P_{avs} will no longer affects P_{out} and so, for a fixed bias, this will lead to a reduction of gain and efficiency (PAE).

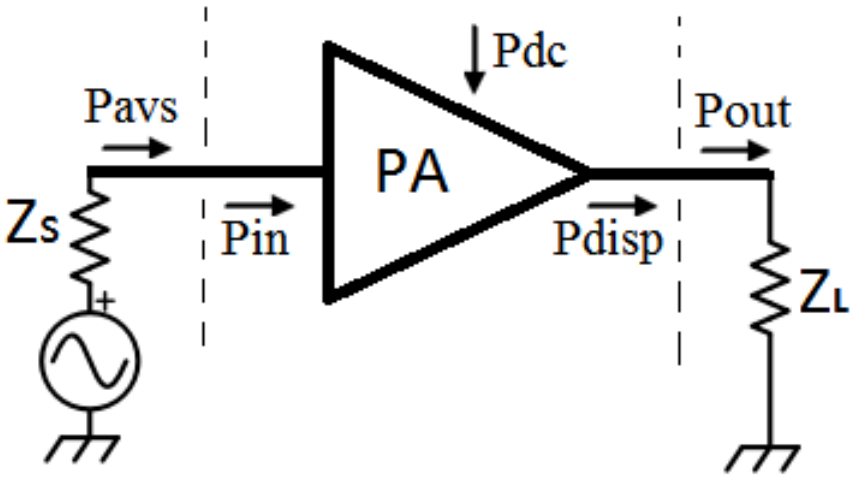

Figure 3 – PA power balance.

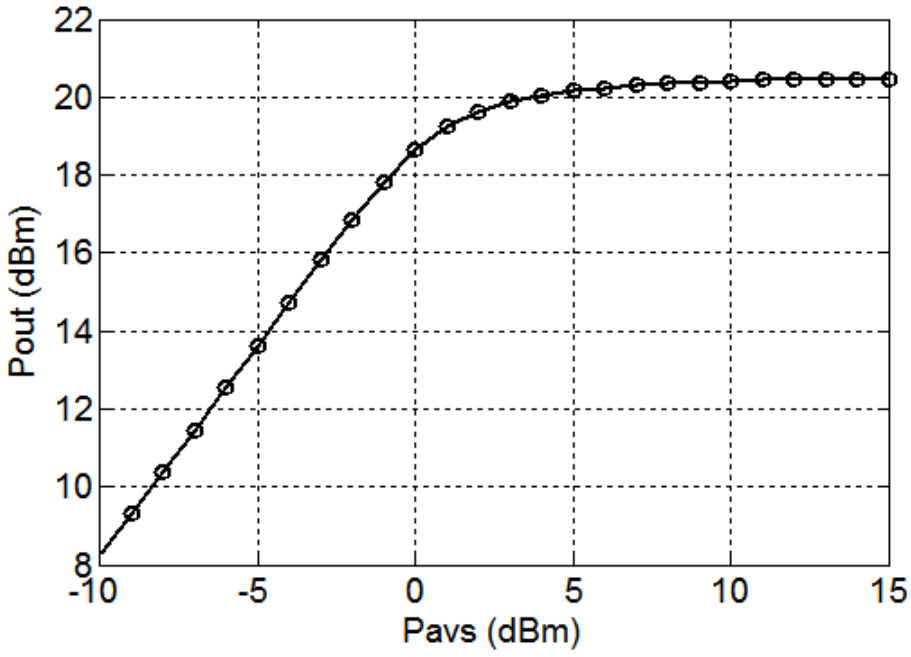

Figure 4 – Output power and saturated output power of an implemented generic PA.

1.1.1.2 Efficiency

Energy consumption is a very important parameter in the design of battery-powered wireless communication systems. The figure of merit that takes this into account is the efficiency. This is why it is one of the main performance parameters of a PA, since most of the energy dissipated in a transceiver occurs in this block. In this way, the power amplifiers must be able to transfer (and amplify) the available power from the source to the load efficiently. Without this, part of the power will be dissipated in the form of heat, causing a temperature increase in the transistor that will result in poor performance or even the burning of the device (worst case). Maximum efficiency is limited by the amplifier class and impacted by the parasitic elements of the circuit. There are two definitions of efficiency: drain efficiency (η) and PAE. The drain efficiency presented in Equation 1.2 describes the relationship between the output power and DC power. Usually, PAE presented in Equation 1.3 is more significant and utilized for taking into account the input power. Through the latter it is noted that for a high gain, i.e. P_{out} much larger than P_{in}, the PAE will be equivalent to drain efficiency.

$$\eta = \frac{P_{out}}{P_{dc}} \tag{1.2}$$

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} \tag{1.3}$$

1.1.1.3 Power gain

There are different power gain terminologies in PAs, due to the impedance mismatches in their input and output. The transducer power gain (Equation 1.4) establishes the relationship between the output power (P_{out}) and the power available by the source (P_{avs}).

$$G_t = \frac{P_{out}}{P_{avs}} \tag{1.4}$$

The operating power gain (Equation 1.5) establishes the relationship between the output power (P_{out}) and the power at the input of the amplifier (P_{in}).

$$G_p = \frac{P_{out}}{P_{in}} \tag{1.5}$$

Finally, the available power gain (Equation 1.6) establishes the relationship between the available power at the output of the amplifier (P_{disp}) and the available power by the

source (P_{avs}):

$$G_{disp} = \frac{P_{disp}}{P_{avs}} \tag{1.6}$$

Transducer gain is the most used because it takes into account all the effects of the mismatches.

1.1.1.4 Linearity

Another important performance parameter of a power amplifier is linearity. This one describes the ability of a PA to amplify the signal with a limited level of distortion. An amplifier responds linearly for small values of power of the input signal. As the signal level grows a variation in the gain arises due to intrinsic non-linearities to the active device. The gain compression occurs when the relation between input power and output power is no longer linear. When the output power is 1 dB less than the expected ideal response, the 1 dB compression point (P_{1dB}) is obtained. This parameter can be referred to input (IP_{1dB}) or output (OP_{1dB}) power. This non-linearity is sometimes also referred as AM-AM (Amplitude Modulation) conversion gain. Graphically this point is obtained by extrapolating the fundamental curve at low input levels and observing where the difference between the extrapolation and the fundamental one is 1 dB (Figure 5).

By plotting the phase of the output signal as a function of the input signal another non-linearity can be observed: the amplitude-phase conversion (AM-PM). This non-linearity causes signal distortion affecting the EVM (Error Vector Magnitude) and the ACLR (Adjacent Channel Leakage Ratio) parameters used to qualify complex modulations. The first one quantifies the error between the output symbol and the reference symbol in a given constellation. A high ACLR will indicate interference in neighboring channels due to the appearance of power side lobes (spectral regrowth).

This work will focus on the measures of 1 dB compression point, because it is the most easy to obtain and used by most works.

1.1.2 Power amplifier operating classes

Power amplifiers are divided into different classes that vary according to the relation between the input and output signal, conduction angle and efficiency. There are four main classes of amplifiers (Class A, B, AB and C) which the active device acts as a controlled current source, also known as sinusoidal class. On the other hand, PAs that use the active device as a switch fit to classes D, E, F and S (among others), also known as switching classes. For these last, the switching frequency must be higher than the operating frequency.

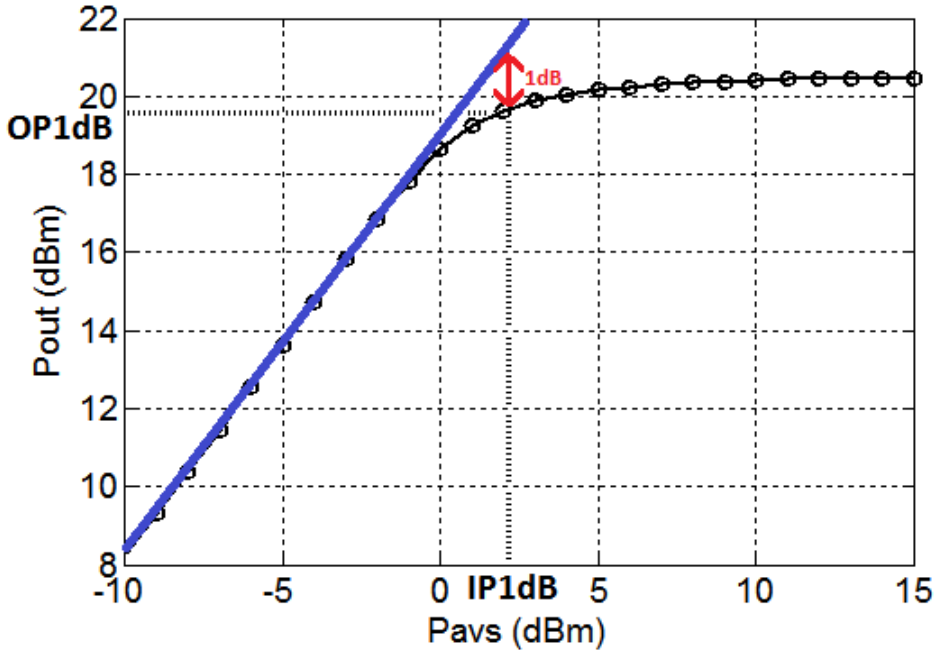

Figure 5 – 1 dB compression point. Black (fundamental), blue (extrapolation).

Therefore, the implementation of these classes at very high frequencies may bring some inconvenience, as the transistor may not switch fast enough (between saturation and cutoff regions). All classes of amplifiers are extensively discussed in (RAZAVI, 2011; LEE, 2004; ROGERS; PLETT, 2010), so here we will address only a brief summary of the conventional classes that use the transistor as a current source.

The class A amplifier is the most linear among all, presenting a 360° conduction angle. The bias of this class is usually established so that the transistor operates (quasi)linearly (LEE, 2004). This condition is satisfied by avoiding cut-off and saturation, in a bipolar transistor. The maximum drain efficiency possible in this class of amplifiers is 50%. As the current conduction angle decreases, linearity also decreases. On the other hand, amplifiers that operate at a reduced angle take the transistor to the cut-off region during part of the cycle, thus increasing efficiency. The class B amplifier is biased so that the transistor is at the conduction threshold. It has a conduction angle of 180° with a maximum theoretical drain efficiency of approximately 78.5%. The class AB amplifier presents a trade-off between linearity and efficiency, since it is biased in order to have a conduction angle between 180 and 360°. The closer to 360° the more linear and less efficient the amplifier will be. The class C amplifier is biased so that the transistor conducts for less than half of a cycle, hence the collector current will consist of a periodic pulse train (if the input signal is also periodic). This class presents a conduction angle between 0 and 180 ° and a maximum drain efficiency of 100%. Table 1 summarizes the classes of amplifiers with their respective conduction angles and drain efficiency. Figure 6 shows the waveform of the collector current in relation to the conduction angle for different classes of amplifiers.

Class	Conduction angle (°)	$\eta_{max}(\%)$
A	360	50
AB	180 - 360	50 - 78.5
B	180	78.5
C	0 - 180	78.5 - 100

Table 1 – Characteristics of the different classes (ROGERS; PLETT, 2010).

It can be seen that the collector current is partially rectified in classes that operate with a conduction angle of less than 360 °. In this way the output must present harmonics that arise because of the effects of non-linearity due to the reduced angle of conduction. These harmonics should be filtered in order to respect the requirements of emission regulators.

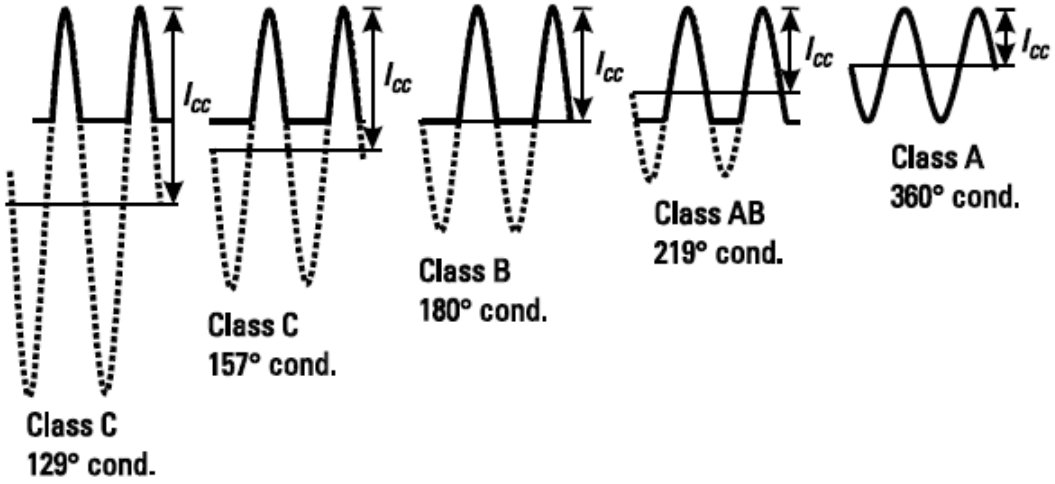

Figure 6 – Current waveforms for various conduction angles (ROGERS; PLETT, 2010).

1.1.3 Power combining techniques

Many times reaching the output power specifications becomes an arduous task in the design of power amplifiers. In the millimeter wave range this work is even more hard, since the gain of a transistor falls with increasing frequency. For this reason, in many of the applications of RF and millimeter waves, it is necessary to use power combining techniques. Two of the most used techniques in millimeter wave PAs are: 1) using transformers and 2) using passive power combining elements, also known as Wilkinson power combiner. Both techniques combine the signals (in phase) of two or more amplifier stages. The transformer combines the voltages in phase so as to achieve a larger excursion of the signal at the output of the PA (Figure 7a).This technique is a good option when the design kit of the technology has integrated transformers. In most technologies, however, integrated transformers are not available. Wilkinson power combiner (or splitter) is another very

interesting technique in high frequency applications, since the length of the transmission lines of its equivalent circuit depends on the wavelength of the signal (Figure 7b). Thus, at high frequencies, this combiner can be integrated into the transceiver chip. This technique allows power combining while providing isolation between ports and impedance matching. Some of the state-of-the-art works of PAs make use of these techniques as we will see in the following subsection.

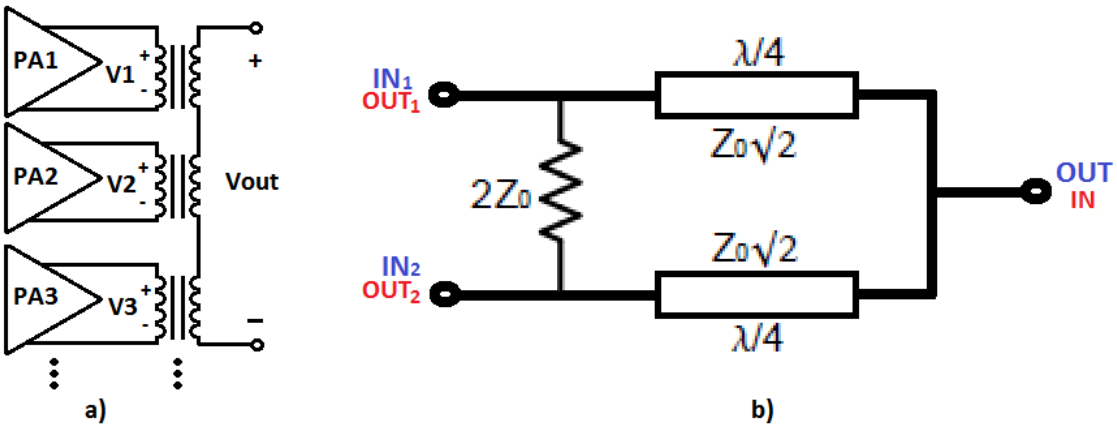

Figure 7 – Power combining techniques: a) using transformer b) equivalent circuit of Wilkinson combiner/splitter.

1.1.4 State of the art in 60 GHz PAs

In this section a review of the state of the art in power amplifier design at 60 GHz band is presented. We considered papers developed in the last decade in SiGe-based processes that vary between 0,25 μm e 0,12 μm. Table 2 summarizes the key performance parameters of these ones. To compare the performance of power amplifiers, in general, a figure of merit (FOM) is adopted, including different performance parameters. One of the ways to define FOM is based on the guidelines introduced by the International Technology Roadmap for Semiconductors (ITRS), which considers the saturated output power (P_{sat}) in dBm, the power gain in dB, the PAE (%) and the central frequency in GHz, defined by (ITRS, 2017):

$$FOM = P_{sat}(dBm) + G(dB) + 10 * \mathcal{L}og(PAE(\%)) + 20 * \mathcal{L}og(fc(Hz)) \tag{1.7}$$

This FOM includes the main performance parameters of power amplifiers. However it does not take into account some others, as the linearity. Sometimes the parameters of Equation 1.7 are used with respect to the 1 dB compression point, but these ones are barely available in published works. For this reason, in order to compare several works, we used the FOM described in Equation 1.7.

Ref	[1]	[2]	[3]	[4]	[5]	[6]	[7]	[8]	[9]
Tec. (μm)	SiGe 0.13	SiGe 0.13	SiGe 0.25	SiGe 0.25	SiGe 0.25	SiGe 0.13	SiGe 0.25	SiGe 0.12	SiGe 0.13
Freq (GHz)	60	60	61	60	60	60	61.5	60	40/ 65
Topology / Architecture	*Push-pull* differ. 1 stage	*Push-pull* differ. 2 stages with power combining by transformer	Cascode *single.* 2 stages	Cascode *single.* 2 stages	Cascode *single.* 1 stage	Cascode *single.* 1 stage	Cascode difer. 1 stage	CE single. 5 stages w/ power combining (2way) wilkinson	Cascode w/ driver (2way) asymmetrical power combining
P_{sat}(dBm)	20	23	15.5	18	14.6	16.8	17.4	21.3	23.6 @55 GHz
$Gain_{sat}$(dB)	4.5	13	14*	11	10.7	11.4	7	22*	18.8 @55 GHz
$Gain_{max}$(dB)	18	20	18.8	15	13.2*	14.5*	14.2	27.5	24*
OP1dB (dBm)	13.1	-	14.5	-	-	11.7	12.2	19.2	19.9 @55 GHz
PAE (%)	12.7	6.3	19.7	14	22	28.4	16.3	14.4	27.7 @55 GHz
FoM	84.60	86.55	82.95	80.02	76.78	81.39	79.49	95.94	96.83
Supply (V)	4	4	3.3	3.3	3	4	3.3	2	4
Pdc (mW)	248	1200	132	198	123	64	257.4	420	-
Area (mm x mm)	1.3 x 0.75	1.9 x 1.8	0.75 x 1.06	0.53 x 0.53	0.61 x 0.56	0.4 x 0.5	0.85 x 0.73	1.8 x 1.3	1.23 x 0.83

* estimated from plots

[1](PFEIFFER; GOREN, 2007a);

[2](PFEIFFER; GOREN, 2007b);

[3](DO et al., 2008);

[4](HAMIDIAN et al., 2010);

[5](HELLFELD et al., 2011);

[6](SUN; FISCHER; SCHEYTT, 2012);

[7](GRUJIC et al., 2012);

[8](YISHAY; ELAD, 2016);

[9](CHAPPID; SENGUPTA, 2017);

Table 2 - State of the art in 60 GHz Power Amplifiers

In the work [1], a single-stage differential cascode circuit was designed to provide a high gain and output power with good efficiency at 60 GHz. A push-pull topology was used for the amplifier core, which is a well known topology implemented at lower frequencies. This topology is used to decrease the impedance transformation ratio required for differential antennas, thereby improving the efficiency of the output matching network. To increase the breakdown voltage of the output device, the cascode were designed very close to each other in order to provide a good AC ground at the base of the output device (common-base). An automatic level detector circuit was also implemented in order to minimize the impacts caused by the variation in process, voltage and temperature (PVT).

In [2] a two-stage amplifier with power combining by distributed active transformers (DAT) was designed. The circuit has achieved a high output power of 23 dBm, which is equivalent to +/- 6.3 V of swing (peak to peak) on a 100 Ω load. The amplifier's core uses a push-pull differential topology very similar to the work [1]. Six Wilkinson power splitters were used to share the signal coming from the driver with the two-stage differential amplifier.

In the work [3], a two-stage single-ended power amplifier was designed to operate at 61 GHz using a 0,25 μm process. The amplifier features a cascode topology operating in AB class providing good gain, isolation and efficiency. Microstrips are used for matching and filtering.

The amplifier in [4] presents a two-stage single-ended cascode topology. The PA core was obtained by optimizing the dimensions of the transistor and by current combination techniques best described in (NATARAJAN et al., 2006). The amplifier can operate in class A and class AB, but the best results of output saturated power and PAE are obtained by operating near the class B region. The matching networks are composed of high quality factor transmission lines and capacitors MIM (Metal Insulator Metal), thus minimizing losses due to matching.

The work developed in [5] presents a methodology to design millimeter wave power amplifiers. This one takes into account the model for small-signals of the active devices, without the need of an accurate model for large-signal. The new methodology was validated by designing a PA in a 0.25 μm process with a cascode, single-ended and single-stage topology. Matching networks were implemented through the use of transmission lines and capacitors.

In [6] a single-ended cascode PA was designed in a 0,13 μm process. A high PAE is obtained by putting the output transistor (common-base) in a weak avalanche region (with an output collector voltage swing close to BV_{cbo}) through its correct sizing. The bias voltages are fixed through the use of HBTs connected as diodes. Linearity is achieved through the optimization of the input network and the degeneration inductor. This PA is the one with the highest PAE and the smallest chip area of all the amplifiers listed.

An one-stage differential cascode power amplifier is presented in [7] using a 0,25 μm process. In this work a careful electromagnetic modeling of the interconnections with the transistors is made. Transmission lines and capacitors are used for matching purposes. The main goal was not to obtain the highest output power and PAE, but rather to show that through a good partitioned and carefully modeled layout, an excellent correlation between simulation and measurement can be obtained.

In work [8] a common-emitter five-stage PA was designed. Two shunt cores are combined in phase through a splitter (at the input) and a modified Wilkinson combiner (at the output). This modified topology is best discussed in (HORST et al., 2007). The power supply of the amplifier is implemented through digitally adjustable biasing circuitry. This PA presents the highest gain among all the amplifiers cited in this section, in addition to presenting the second largest FOM.

The most recent paper found [9] was published by August 2017. A new methodology for impedance synthesis is discussed. Amplifiers feature a cascode topology in parallel preceded by drivers. Each branch are summed through an asymmetric combiner, which allows the programmable synthesis of complex impedances. This allows the cores to see the optimal output impedance, thus relieving trade-offs between output power, efficiency and frequency reconfigurability. The PA features a 25 GHz operating band between 40 and 65 GHz, with best results at 55 GHz. This work was the one that presented the highest saturated output power and FOM among those summarized in Table 2.

In this work, we followed the line of work [6], which allows to obtain good results of Pout and PAE, through taking the transistor to a weak avalanche region. This was designed without the use of power combining techniques, greatly reducing the used chip

area (which is also a constraint). On the other hand, the design-kit of the technology has power combiners, however these would only be used if we could not meet our output power specifications with a single amplifier, as the power consumption and the area would increase. The layout-oriented approach proposed in this thesis also recalls what was done (layout partitioning) in work [7].

1.2 The 60 GHz band

The growing demand for wireless communication devices and the need of higher speed rates, makes relevant and necessary the use of the spectrum in the millimeter wave range. According to the channel capacity theorem proposed by Shannon Hartley (Equation 1.8), one of the ways to achieve a higher data rate is through the use of a larger band.

$$C = Band * \mathcal{L}og_2(1 + SNR) \tag{1.8}$$

where C is the channel capacity (in bits/s), Band is the bandwidth (in Hz), and SNR represents the signal-to-noise ratio (linear power ratio).

The sub-6 GHz spectrum is already saturated by existing several communications standards. Millimeter wave range then becomes the most attractive option to obtain gigahertz bandwith, allowing a high data rate. Within the spectrum of millimeter waves, the band around 60 GHz is one that attracts most the industry's attention in the world for the next generation (5G) mobile systems. This is due the fact this is a band not yet licensed in most part of the world. In the United States of America this band is ranged between 57 and 64 GHz, as well as in Canada and South Korea. In the European Union this band extends from 57 to 66 GHz, whereas in Japan it is between 59 and 66 GHz. In Brazil, however, the band between 57 and 64 GHz has already been licensed for satellite applications, while the band between 64 and 71 GHz remains unlicensed (TELECO, 2017; ANATEL, 2017). Figure 8 presents a summary of the unlicensed spectrum around the world.

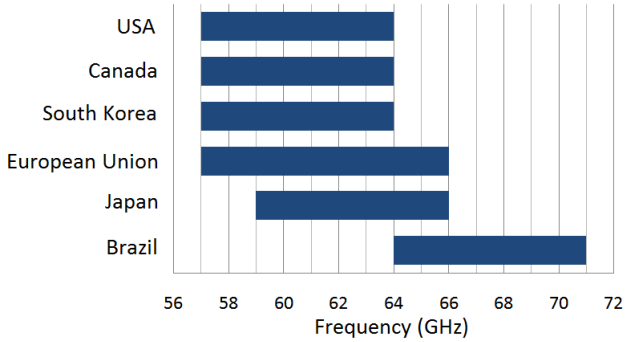

Figure 8 – Unlicensed frequency bands near 60 GHz around the world.

The allocation of frequency bands to the next generation of mobile (5G) systems, however, will only really be defined by the ITU (International Telecommunication Union) during the World Radiocommunication Conference (WRC), which will take place in 2019. There is a strong tendency for the band around 60 GHz to be one of the chosen, and the whole world industry uses it, including Brazil. In addition to being unlicensed, the 60 GHz band presents some peculiarities that have aroused great interest for short-range wireless networks. The oxygen absorption at this band generates a high attenuation of the signals that cross the environment, making it ideal for dealing with a dense and secure data traffic. Figure 9 shows this attenuation as a function of frequency. In 59.755 GHz one of the attenuation peaks occurs, with a value equal to 15.255 dB/km (YILMAZ; FADEL; AKAN, 2014). This attenuation is an advantage when it is desired to transmit data in a safe way, since the waves will not propagate for long distances. Interferences with other standards operating in the same frequency range will also be minimized because of this. In this way the main applications of this band will be focused on the Wireless Local Area Network (WLAN) and Wireless Personal Area Network (WPAN). In addition, the small wavelength in this frequency range allows the miniaturization of the antennas, allowing them to be integrated in the same chip of the transceiver.

The 5G generation will also make use of the concept of small cells that was already introduced in 4G. This cell is basically a miniature of a base station that breaks up a cell site into much smaller pieces (pico cells, micro cells and femtocells), with applications for indoor and outdoor systems. Small cells are typically used in very densely populated urban areas for improving coverage and signal strength. This concept is not fully matured, but has undergone a great evolution in the last years, through the development of new techniques that minimize its disadvantages.

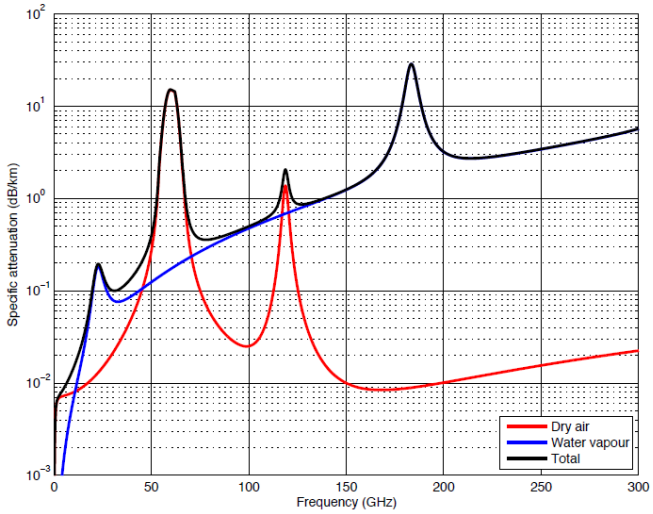

Figure 9 – Specific attenuation due to atmospheric gases as a function of frequency (YILMAZ; FADEL; AKAN, 2014).

1.2.1 Standards

Due to the great opportunities that this frequency range can offer, there is a joint effort of the international industry to standardize and commercialize it (RAPPAPORT et al., 2011). Some standards are already well matured and are constantly updated by the technical groups. Some of these are: ECMA-387 , WirelessHD, 802.15.3.c (TG3c) and WiGig.

1.2.1.1 Wireless HD

The Wireless HD standard is a consortium created among giants of the electronics industry, some of them: Intel, LG, Samsung, Sony, Toshiba and others. This consortium is dedicated to providing a unified standard, based on the 60 GHz spectrum, for high-speed wireless communication of electronic products. Its specifications were made available in 2008. The main applications of this standard are turned to wireless transmission of lossless high-definition audio and video, creating the so-called Wireless Video Area Network (WVAN). Its current data rate is between 10 and 28 Gb/s (WIRELESSHD, 2017).

1.2.1.2 ECMA-387

The European Computer Manufacturers Association (ECMA) has also set a standard since 2010 at this band. The ECMA-387 is intended to support a massive transfer of data, such as data downloads and high-definition multimedia streaming (ECMA, 2017).

1.2.1.3 IEEE 802.15.3.c (TG3c)

The IEEE 802.15.3 TaskGroup 3c (TG3c) standard was formed in 2005 to develop a Physical Layer (PHY) alternative in the millimeter wave band for the WPAN 802.15.3-2003 standard. This standard supports high speed rate for applications such as: high speed internet access, streaming, among others. (IEEE, 2017).

1.2.1.4 WiGig

The Wireless Gigabit Alliance (WiGig) standard was announced in 2009 promoting the already existing IEEE 802.11ad protocol, with applications aimed at extending computer peripherals and high definition interfaces, such as projectors and monitors. In 2013, WiGig was acquired by the Wi-Fi Alliance. In 2016 the Wi-Fi group introduced the certificate so-called "Wi-Fi CERTIFIED WiGig™", in order to accelerate the commercialization of the WiGig devices (WIFI, 2017). WiGig will enable service providers to use millimeter wave spectrum for point-to-point connectivity as an alternative to fiber. Facebook has

announced recently multiple new partnerships to bring the concept of Terragraph (in essence are WiGig radios forming a city mesh) to market, delivering fiber-like speeds and high-capacity connectivity to dense urban areas. The idea is to use the huge amount of spectrum available in 60 GHz to connect city people to a faster, better, and cheaper Internet (WIFI, 2018). Operating in this less crowded frequency band, this standard enables extremely high performance, multi-gigabit connectivity and low latency for a range of applications, including wireless docking, augmented reality/virtual reality (AR/VR), multimedia streaming, gaming, and networking. (WIFI, 2017)

All of these standards operate in the unlicensed band around 60 GHz (57 to 66 GHz). This 9 GHz free spectrum is generally divided into four channels with 2.16 GHz each. The most commonly used modulation techniques are Single Carrier (SC) and Orthogonal Frequency Division Multiplexing (OFDM).

1.3 Microwave Theory

At high frequencies, the standard circuit theory cannot be used directly to solve circuits. This is due to the fact that this is an approximation of the broader electromagnetic theory, also known as Maxwell's equations. The theory of transmission lines bridges the gap between field analysis and classical circuit theory, becoming an extremely important tool for the analysis of microwave networks. (POZAR, 2005).

1.3.1 Transmission lines: model and propagation

The classical circuit analysis considers that the wavelength of the signal is much larger than the physical dimensions of the devices, characterizing them as lumped circuits. When this condition is not satisfied the circuits are considered to be distributed, where the voltages and currents can vary significantly in magnitude and phase over the phsyical extent of the device. In Figure 10 the schematic of a two-wire transmission line is presented. The infinitesimal line of length $\triangle z$ can be modeled by a circuit with lumped elements, shown in Figure 10b.

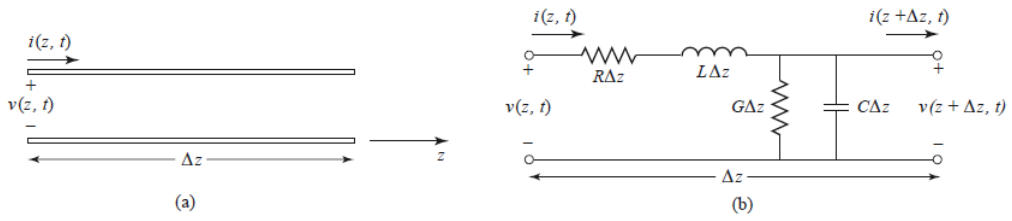

Figure 10 – Equivalent circuit for an incremental length of transmission line (POZAR, 2005).

The parameters R, L, G and C are per unit length quantities. The series resistance (R) represents the resistance due to the finite conductivity of both conductors and is expressed in Ω/m. The inductance (L) represents the self-inductance of both conductors in H/m. The parameter C represents the shunt capacitance due to the proximity of the two conductors (in F/m), while G represents the conductance due to the dielectric losses in the material between the conductors (in S/m). A finite transmission line can be seen as a cascade of several sections of the circuit of Figure 10b (POZAR, 2005). However, there is a difficulty in working with transmission lines on a silicon substrate due to the relatively high doping (high G) of this, which introduces significant transmission losses and limits the quality factor of these lines.

1.3.2 Scattering parameters (S-parameters)

The scattering parameters (or S-parameters) are used to characterize the behavior of linear systems at high frequencies, where obtaining other parameters through measures becomes more complex (RAZAVI, 2011; LEE, 2004). A diagram of the representation of the S parameters for a two-port network is shown in Figure 11.

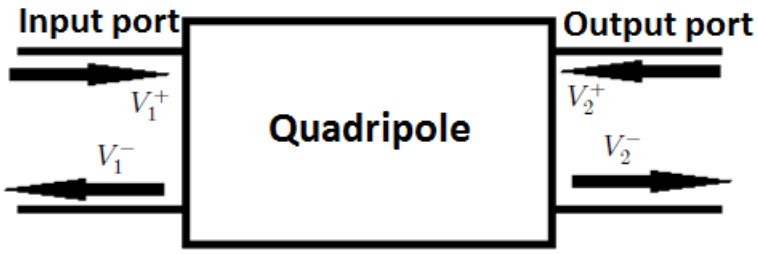

Figure 11 – Representation of the S parameters in a quadripole.

The main idea of this representation is to measure the incident voltage wave V_1^+ entering the system, as well as the corresponding reflected voltage wave V_1^- coming out of the system (through the input port). The incident and reflected normalized waves V_1^+ and V_1^- are related to the terminal voltages and currents of the input port. For the network shown in Figure 11, contributions from the two ports can be combined to form the Equation 1.9 in the matrix form.

$$\begin{bmatrix} V_1^- \\ V_2^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \end{bmatrix} \tag{1.9}$$

where S11, S12, S21 and S22 are the scattering parameters measured between the input

and output port. Expanding the scattering matrix, the following equations can be written:

$$S_{11} = \frac{V_1^-}{V_1^+}, if \rightarrow V_2^+ = 0 \tag{1.10}$$

$$S_{12} = \frac{V_1^-}{V_2^+}, if \rightarrow V_1^+ = 0 \tag{1.11}$$

$$S_{21} = \frac{V_2^-}{V_1^+}, if \rightarrow V_2^+ = 0 \tag{1.12}$$

$$S_{22} = \frac{V_2^-}{V_2^+}, if \rightarrow V_1^+ = 0 \tag{1.13}$$

where S11 is the input reflection coefficient (input impedance), S12 is the reverse transmission coefficient, S21 is the forward transmission coefficient and S22 is the output reflection coefficient (output impedance) of a quadripole. These parameters are widely used in low noise amplifier designs, impedance matching and stability criteria analysis.

1.3.3 The Smith chart

A very useful way of graphically visualizing impedances is through the Smith chart. This allows you to trace impedances with the real part between zero and infinity and with any possible imaginary values. Using the concepts of reflection coefficients, it is possible to measure how well two impedances are matched. The voltage reflection coefficient (Γ) is defined by the amplitude of the reflected voltage wave normalized with respect to the amplitude of the incident voltage wave:

$$\Gamma = \frac{V_0^-}{V_0^+} = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{1.14}$$

where Z_0 is the characteristic impedance and Z_L is the load impedance.

Rewriting Equation 1.14, it can be defined the load impedance in the following way:

$$Z_L = Z_0 \frac{1 + \Gamma}{1 - \Gamma} \tag{1.15}$$

The real impedances are represented between $0\Omega(\Gamma = -1)$ to $+\infty\Omega(\Gamma = +1)$, so when $\Gamma = 0$, $Z_L = Z_0$. This means that the center of the Smith chart indicates the point at which the load is identical to the characteristic impedance (i.e., matching condition). Normalizing with respect to Z_0, one can obtain the impedance directly from the Smith chart of Figure 12. The circular lines represent the constant resistance contour, whereas

the arc lines correspond to the constant reactance. In addition the upper part of the chart represents positive reactance (inductive), while the lower one negative reactance (capacitive). In the chart of Figure 12, we represent the points A and B, which are impedances that will be used further in this work for matching purpose.

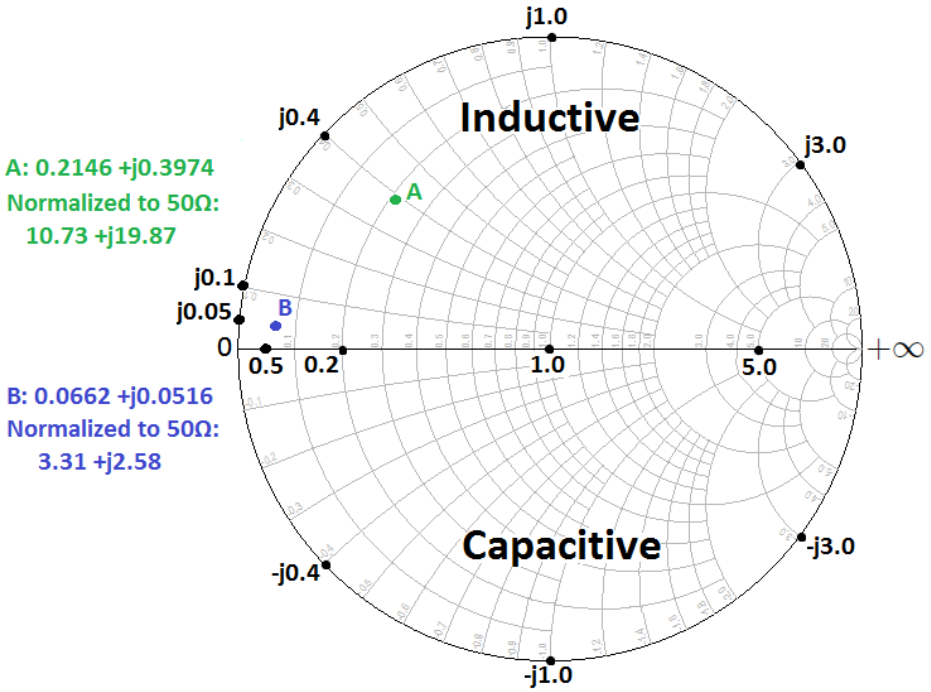

Figure 12 – Smith chart. Points A and B are two examples of impedances in the chart.

1.4 Stability analysis criteria

An important feature of amplifiers is stability analysis. Through this, it can be ensured that oscillations will not occur due to the presence of feedback paths from the output to the input, that might arise (oscillations) for certain combinations of input and output impedance. For this analysis under small-signal operation consider the circuit of Figure 13.

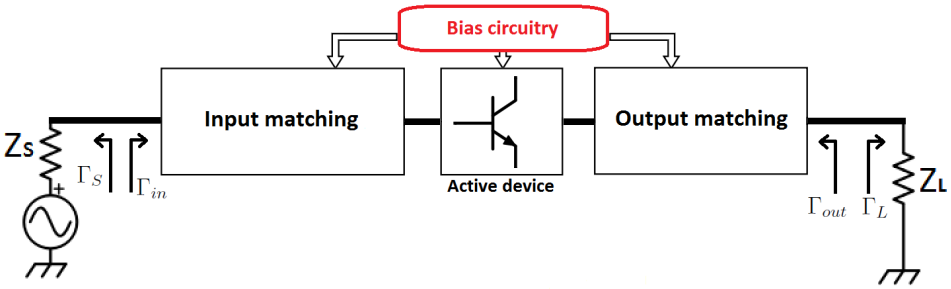

Figure 13 – Circuit for stability analysis.

Considering this circuit, oscillations are possible when the impedance of the input or output port presents negative real part, implying in: $|\Gamma_{in}| > 1$ ou $|\Gamma_{out}| > 1$. It is worth remembering from the subsection previous that a reflection coefficient greater than unity indicates a region outside the Smith chart. Because Γ_{in} and Γ_{out} depend on the input and output matching networks, the stability of the amplifier will also depend. In (POZAR, 2005) two types of stability are defined:

- Unconditional Stability: The network will be unconditionally stable if $|\Gamma_{in}| < 1$ e $|\Gamma_{out}| < 1$ for any passive load and source impedances (i.e., $|\Gamma_S| < 1$ and $|\Gamma_L| < 1$)
- Conditional Stability: The network will be conditionally stable if $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$ only for a certain range of passive load and source impedances. This case is also referred to as potentially unstable.

The stability criteria of the amplifiers are usually frequency dependent, since the input and output matching networks generally are too. In this way it is possible that the amplifier is stable in the operating frequency, but becomes unstable in other ones. Therefore the criteria must be evaluated over a wide spectrum range in order to ensure stability. There are several ways to test the stability conditions of a circuit. One is to determine regions on the Smith chart for Γ_s and Γ_L where the amplifier is conditionally stable. This approach requires a more elaborate mathematical treatment that can be seen in detail in (POZAR, 2005). On the other hand, there are simpler tests to be evaluated that determine the unconditional stability of the circuit using the S parameters, known as the Rollet's stability factor (K and Δ), and defined as follows:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2\,|S_{12}S_{21}|} \tag{1.16}$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| \tag{1.17}$$

When $K > 1$ and $|\Delta| < 1$ are simultaneously satisfied, they form a set of necessary and sufficient conditions for unconditional stability (POZAR, 2005). If these conditions are not met stability circles should be used to determine if there are Γ_s and Γ_L values for which the circuit is conditionally stable. Despite the K and Δ parameters form a rigorous mathematical treatment to indicate unconditional stability, they do not serve to compare the stability of different devices, that is, it does not indicate how good the stability of one circuit relative to another is. This is due to the need to meet two different requirements (K and Δ). An alternative method proposed in (EDWARDS; SINKSY, 1992), known as

geometric stability factor, uses only one requirement to indicate stability, the parameter µ defined below.

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12} - S_{21}|} \tag{1.18}$$

For $\mu > 1$ the amplifier will be unconditionally stable. The geometric stability factor calculates the distance from the center of the Smith chart to the nearest point of instability. In this way higher values of μ indicate a better stability. The parameters K, Δ and μ are sufficient to prove and qualify the stability of a device. Sometimes in Computer Aided Design (CAD) tools the K parameter is made available directly in the setups of S-parameter simulations, whereas the Δ is not. In these cases there is another parameter also widely used to replace the Δ, known as factor B1 and defined by:

$$B1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \tag{1.19}$$

If $K > 1$ and $B1 > 0$ the circuit will be unconditionally stable.

These criterias considers that the circuit works with small-signals (only powered), also known as stationary analysis. Under large-signal operation, however, the stability analysis is a much more harder task. One approach is to use the Poles and Zeros (PZ) analysis, but first, it is necessary to put the amplifier in a known non-linear state (by applying an input signal that does it). Then small-signal PZ analysis is performed around this non-linear operating point. This is a hard task because this non-linear stability analysis needs to be conducted at several drive conditions (frequency-power level set). In addition, this PZ analysis works well only for small networks (EDWARDS, 2012). One example of PZ identification tool is STAN (AMCAD, 2018).

Another approach is to use network-system identification routine by applying a dataset obtained through circuit analysis in the real frequency domain. These routines tend to be focused on the pure mathematical manipulations rather than the analysis of electronic circuits(EDWARDS, 2012).

1.5 Impedance matching

The impedance matching seeks to minimize reflection between a source and a load. In other words, it targets maximize power transfer. There are two approaches to impedance matching analysis. When designing circuits that work with small-signal levels, such as the LNA, the small-signal approach is utilized. In this approach one can determine the three different types of power gains (Equations 1.4, 1.5 and 1.6) in terms of the S parameters and the reflection coefficients (Γ_s e Γ_L). These gain definitions differ mainly by how the source

and the load are matched to the circuit. The most useful one is the gain of the transducer (G_t), because it takes into account both source and load mismatches. In the condition that the input and output are the conjugate complex of the source and load impedances respectively, the power gain will be maximized and thus $G_t = G_p = G_{disp}$(POZAR, 2005). In the design of power amplifiers the small-signals analysis can not be considered, since the device is usually driven to a non-linear region of operation. In PAs the requirements to maximize the output power of the amplifier usually differ from those used to maximize power gain in small-signals. Under these conditions the optimal source/load impedances may no longer correspond to the conjugate complex of the input/output impedances. The optimum load impedance value for a maximum output power is found through load-pull measurements and/or simulations. This approach will be discussed in the following subsection, whereas the analysis in small-signals can be well evaluated in (POZAR, 2005; RAZAVI, 2011).

1.5.1 Large-signal impedance matching (Load-Pull)

To evaluate the effect of the load impedance on the power delivered to it, load-pull approach is used. This allows to systematically vary the real and imaginary parts of the load impedance, so as to trace constant power contours in the abacus of the Smith chart (LEE, 2004). This set of contours are known as a load-pull diagram. This approach is used in non-linear analysis (e.g. for PAs), since in the linear analysis there are much simpler and faster methods (both in simulation and measurements), which already produce satisfactory results. The derivation of the analytical approach of this method was first proposed in (CRIPPS, 1983) for a PA in GaAs. The method by simulation consists of the addition of a tuner connected between the transistor output and the load. The tuner is configured to synthesize a wide range of impedances to be viewed at the output of the transistor, while the source remains as the conjugate complex of the input impedance. The latter is determined to be the voltage-current relationship of the input observed at the frequency of interest and at the point of maximum output power. In this analysis can be obtained the behavior of some of the key performance parameters of a PA for a wide range of synthesized impedances. In addition to the power contours, others like the PAE are also important to be analyzed. Figure 14 shows an example of a load-pull diagram for output power and PAE of a bipolar transistor of the technology used. As can be observed this analysis resembles contour lines, where the highest values are concentrated more to the center of the contours. Figure 15 shows the load-pull diagram under different input signals levels. As can be seen, the optimal output impedance in large-signal (red) differs from that small-signal (green) ones. So, the requirements to maximize the output power of the amplifier differ from those used to maximize power gain in small-signals.

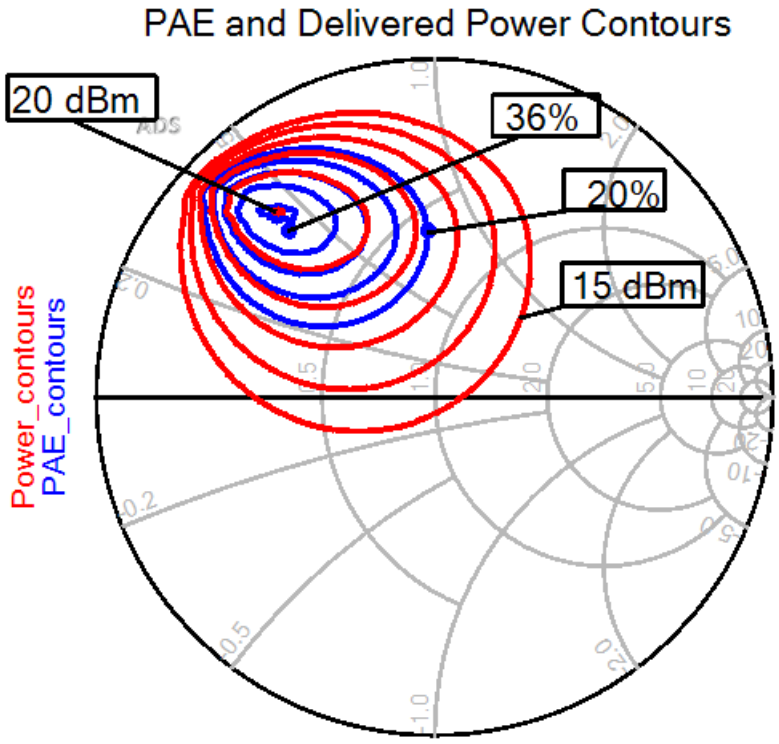

Figure 14 – Load-pull diagram for a bipolar cascode topology. Output power in red and PAE in blue.

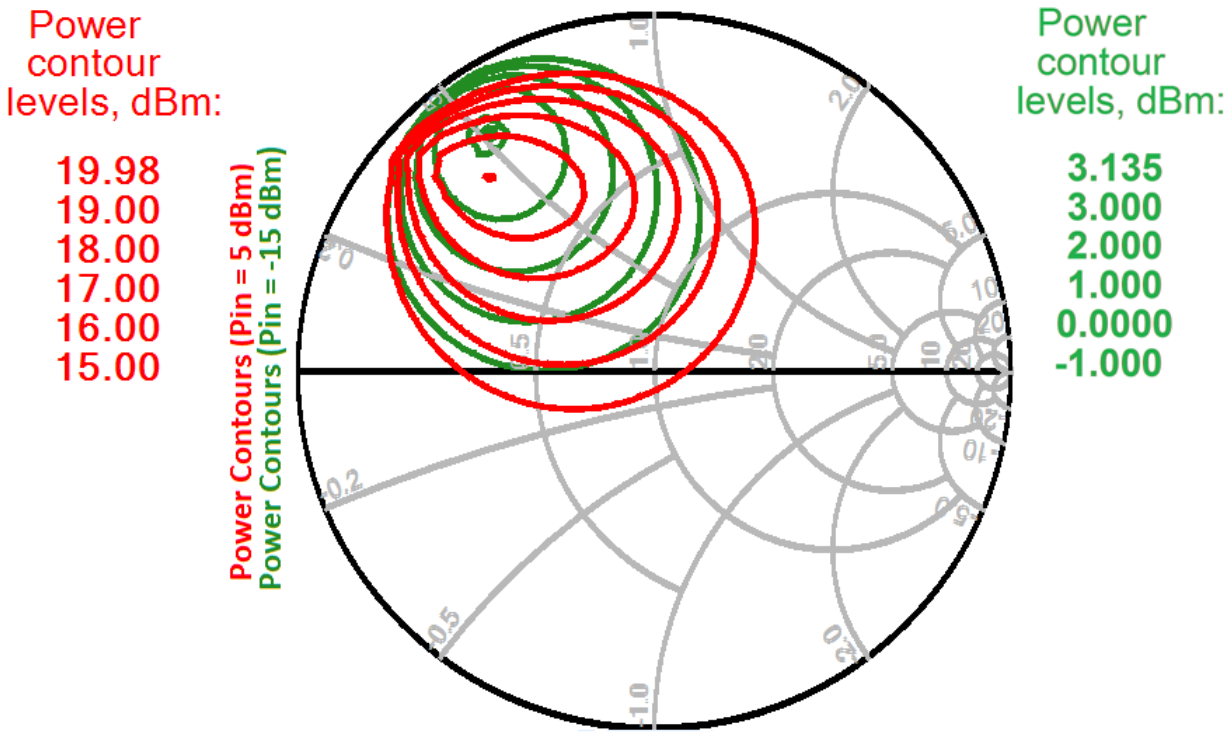

Figure 15 – Load-pull diagram for a input level of -15 dBm (green) and 5 dBm (red).

1.5.2 Synthesis and impedances transformation

From the moment that the load and source impedances are already determined, it is necessary to synthesize the matching network that will provide these ones. This can be accomplished through analytical methods or through the use of the Smith chart. For the analytical case there are some impedance matching networks most commonly used, they are: matching section in L , in T and in π. The most simple and common of these ones is the matching network in L. In (RAZAVI, 2011; POZAR, 2005) a detailed treatment about it can be obtained. On the other hand, the Smith chart provides a visual, fast and powerful tool to synthesize matching networks, which can be optimized with the aid of a CAD tool. These networks are constituted in a series and parallel impedance alternation. Any impedance (or admittance) can be transformed by moving along the constant circles of resistance and conductance, through the use of capacitive and inductive elements. The addition of ideal components in series causes a movement along the circle of constant resistance, changing only its reactance. On the other hand the addition of ideal shunt components causes a movement along the circle of constant conductance (Figure 16a). The graphical approach is the most commonly used in RF designs, because it is intuitive and allows the results to be refined quickly and simply in CAD tools by tuning. Figure 16b shows an example of how to synthesize an impedance (which will be used further in this work for matching purpose) using ideal components. This latter parts from a impedance of 50Ω (red dot), which is in general the load and source impedances of the systems.

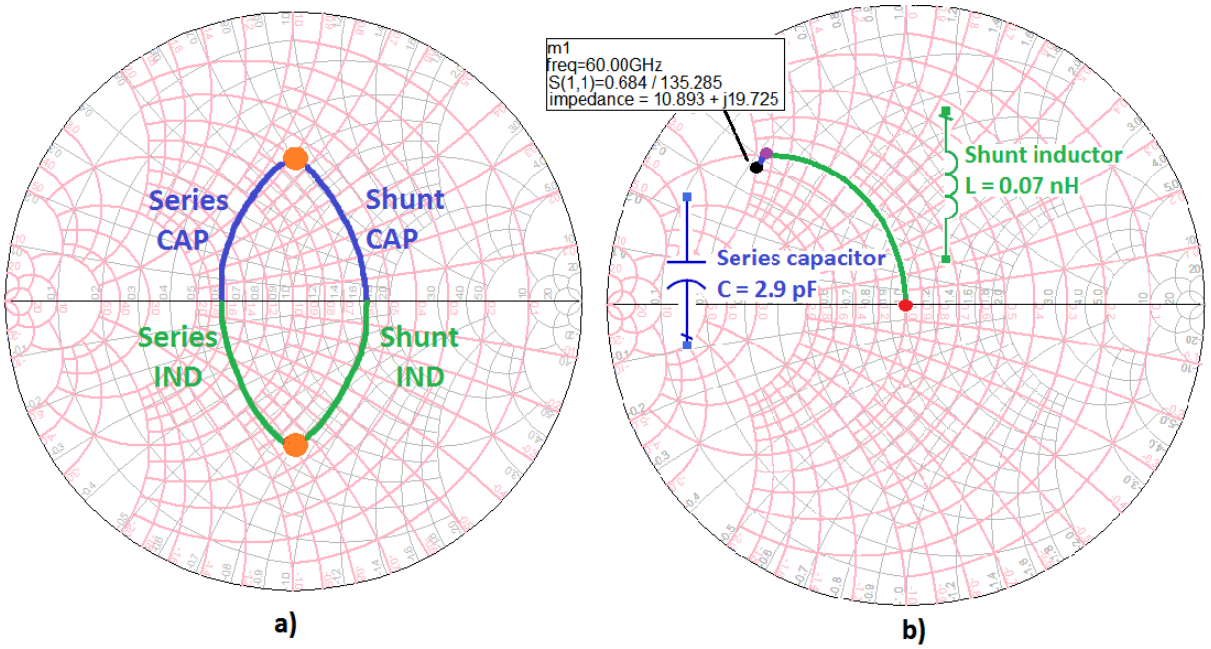

Figure 16 – a) effect of the addition of capacitive and inductive ideal components on the Smith chart. b) example of an impedance synthesis at 60 GHz using ideal components.

2 A Brief Introduction to Some Elements Available in BICMOS8HP Technology

A homojunction is a structure formed by the same semiconductor materials (e.g. Silicon), which have the same bandgap, but with different doping. This structure is the basis of a pn junction, such as diodes and Bipolar Junction Transistors (BJT). On the other hand, a heterojunction (or heterostructure) is a sequence of at least two layers of different semiconductor materials (e.g. Silicon and Germanium) with distinct bandgaps grown epitaxially one on top of the other. The heterostructures are the main component of the todays most advanced high frequency and high performance transistors such as High Electron Mobility Transistors (HEMT) and Heterojunction Bipolar Transistors (HBT) (SCHWIERZ, 2000).

In a homojunction Silicon bipolar transistor, electron transport across the base is primarily done by diffusion, which is a relatively slow process. The base region is, in most Silicon bipolar process, formed by implantation, resulting in a somewhat retarding field for electrons (IBM, 2011). By varying the base composition a graded bandgap can be obtained that causes an accelerating base field, decreasing the base transit time and thus increasing the transition frequency (f_t) (SCHWIERZ, 2000). This last parameter is defined as the frequency for which the current gain equals unity and output is AC shorted, also known as cut-off frequency. The maximum oscillation frequency, f_{max}, is often a more important parameter than f_t in real circuits. It is the frequency at which maximum unilateral power gain equals unity. Both parameters are used to qualify high frequency performance of transistors. At low currents, f_t improves linearly with current density. When the current density is high enough such that the minority carrier density is comparable to the collector doping concentration, the effective base width increases and the device becomes slower (Kirk effect). Higher collector doping concentration is desired because it moves the onset of the Kirk's effect to a higher current density (indicating a higher f_t) (IBM, 2011). On the other hand, it lowers the collector base breakdown voltage. So, there is a trade-off between f_t and breakdown voltages, as both have a strong dependence on collector doping.

The addition of Germanium in BiCMOS8HP technology results in a reduction of the bandgap, of approximately 74 meV per 10 % of Germanium content. A higher concentration of Ge will imply an inclination of the conduction band, acting as an accelerating field for the minority carriers in the base. Due to this drift field, the electrons will move quickly through the base, indicating in a lower base transit time. This is key to improving the device speed compared to all Silicon homojunction bipolars. The graded Ge concentration also improves current gain and Early voltage (output conductance) compared to a Silicon homojunction transistor (IBM, 2011). All these factors make the SiGe-based transistor

better than those made only of Silicon for operation in very high frequencies.

The main benefits of using a Silicon substrate are the easy integration with other circuits (analog, RF and digital) and the low cost of the process. In this sense, the SiGe-based process represents a middle-ground between the silicon-based processes and those based on group III-V (GaAs, GaN e InP), in terms of performance in high frequencies and integration. As already mentioned, the technology used in this work is GF SiGe BiCMOS8HP of 0.13 μm , which has a BEOL (Back-end-of-line) between 5 and 7 layers of metals. The available one was the 7-metal layer process, offering two thick 1.25 μm and 4 μm Aluminum top layers for low loss interconnects and high-performance transmission lines. This stack layer is shown in Figure 17. Capacitors, inductors, transmission lines and interconnections make use of the top Aluminum layers. The other layers are made of copper, MQ layer being the thickest and M1 the thinnest. The transistors are at the level of the substrate with accesses to the M1 metal. The subsection following will briefly cover some of the available components in this technology.

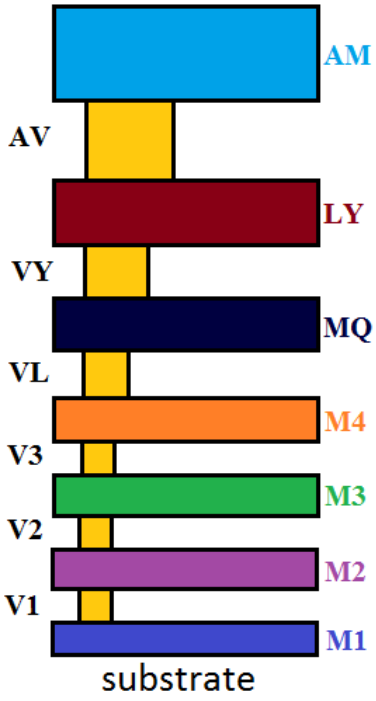

Figure 17 – BiCMOS8HP metal layers.

2.1 The HBT transistor (npn)

As already discussed, the heterojunction bipolar transistor (HBT) presents best performance when compared to traditional bipolar transistors. This technology features two different HBT transistors: one with a higher transition frequency and the other one

with a higher breakdown voltage. The first one features a transition frequency of 200 GHz, while the other of only 57 GHz. Due the goal of this work was to design 60 GHz amplifiers, the one with the highest transition frequency was chosen. In addition, this device has two different configurations. One of them has a single access to the collector, base and emitter (CBE transistor), while the other has only one access for the emitter, however, it has two for the collector and the base (CBEBC transistor). The one with two accesses is the most recommended configuration by the manufacturer, from a performance and reliability perspective, at the cost of a relative larger area. Figure 18 shows the layout of the CBEBC configuration. All accesses are by M1 metal.

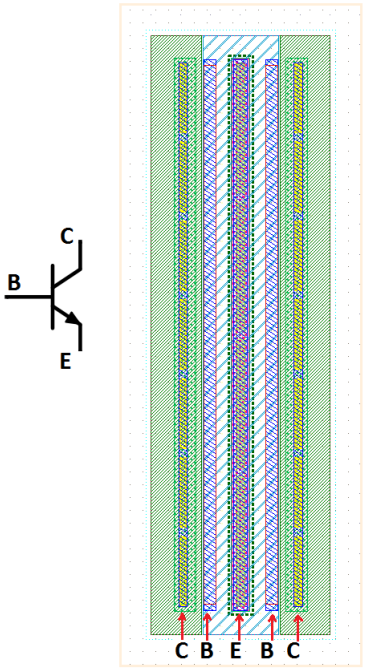

Figure 18 – Transistor HBT (18μm) npn CBEBC.

The NPNs have fixed emitter (single stripe only) width of 0.12 μm. These NPNs provide the lowest base resistance for low noise operation. The emitter length may be selected from 0.52 to 18μm. This restriction exists to avoid a long signal-path and inconvenient geometries design. For configurations that require larger emitters, the multiplicity parameter can be used. These transistors have a transition frequency (f_t) of 200 GHz and a maximum oscillation frequency (f_{max}) of approximately 280 GHz (IBM, 2011). The breakdown voltage between the collector and the base (BV_{cbo}) is approximately 5.5 V (PFEIFFER; GOREN, 2007a), while the breakdown voltage between the collector and the emitter (BV_{ceo}) is approximately 1.8 V (IBM, 2011). Additionally this transistor has a current density at the peak of f_t of approximately 12 mA / μm^2. To analyze its ability to provide gain at 60 GHz, its maximum available gain (GMAX) is extracted from S-parameters simulations at various bias conditions. Figure 19 shows the dependence of GMAX on the bias current of a HBT transistor with a emitter length (exl) of 18 μm and

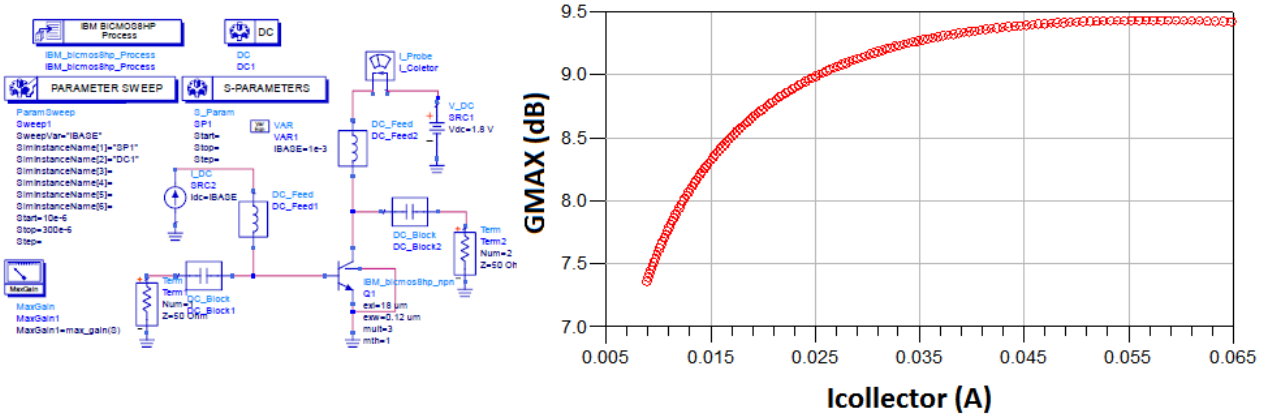

Figure 19 – GMAX of HBT (CBEBC), VCE = 1.8 V.

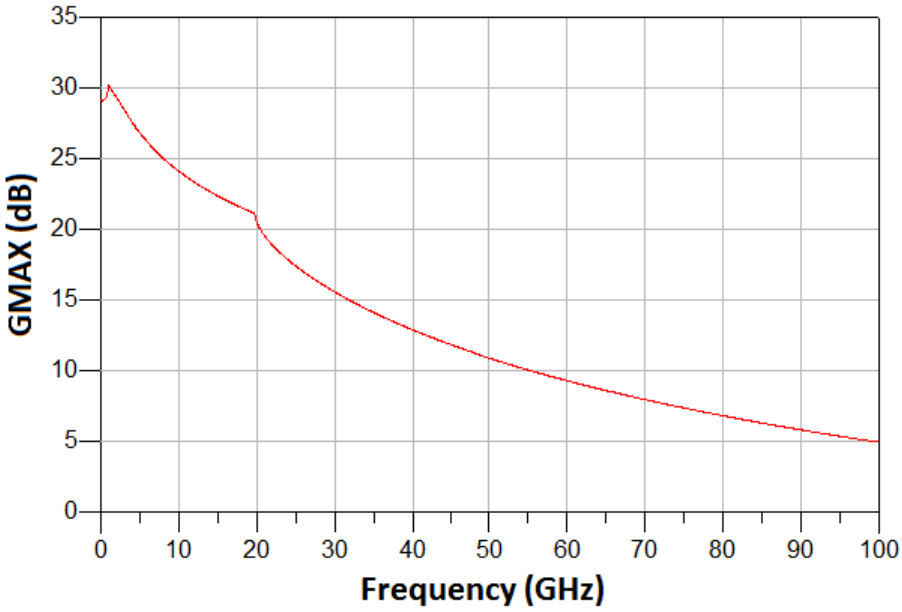

Figure 20 – GMAX as a function of frequency at 60 mA.

a multiplicity of 3. For a collector bias current of 60 mA, a common-emitter transistor can already provide a gain of 9.43 dB, and the gain saturates for higher values of bias currents. Figure 20 shows the dependence of GMAX (with 60 mA of collector current) as a function of frequency.

2.2 Resistors

This technology presents some options for resistors, two of which are shown in Figure 21.

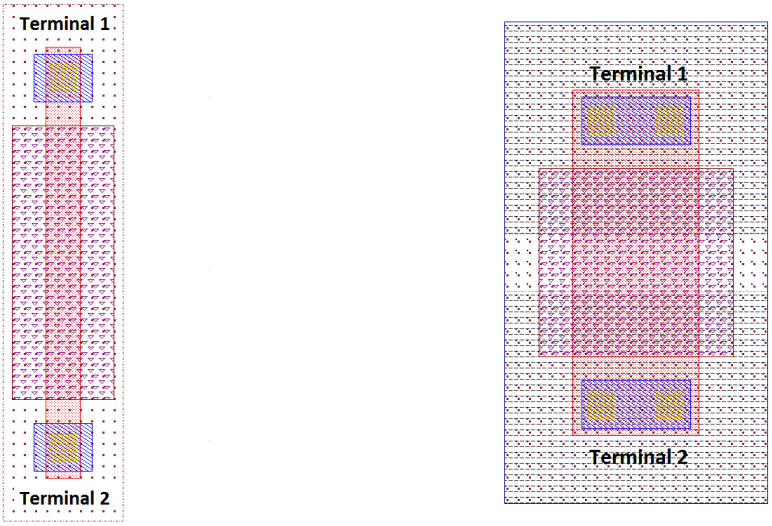

Figure 21 – Opppcres (3.694 kΩ) and oprrpres (991 Ω) resistors.

The opppcres resistor has a lower sheet resistance and tolerance, being used when small resistances are required. On the other hand the oprrpres has a higher sheet resistance and tolerance. This will be used in situations where high resistance is required. Both are made of polysilicon and are built below the M1 metal. Only rectangular geometries are allowed. The terminals are accessed by M1 metal.

2.3 Capacitors

There are two options of metal-insulator-metal (MIM) capacitors available in the technology and presented in Figure 22. The MIM and dualMIM capacitors have a scalable rectangular geometry with capacitances ranging from tens of fF to tens of pF. For an identical area, the dualMIM has a higher capacitance. MIM capacitors were used for matching purposes because they present, for an identical capacitance, a lower real impedance. The dualMIM capacitors were used where was needed large capacitances. Both are built between the outermost layers of aluminum (AM and LY). Figure 23 shows the behavior of these capacitors as a function of frequency in the Smith chart.

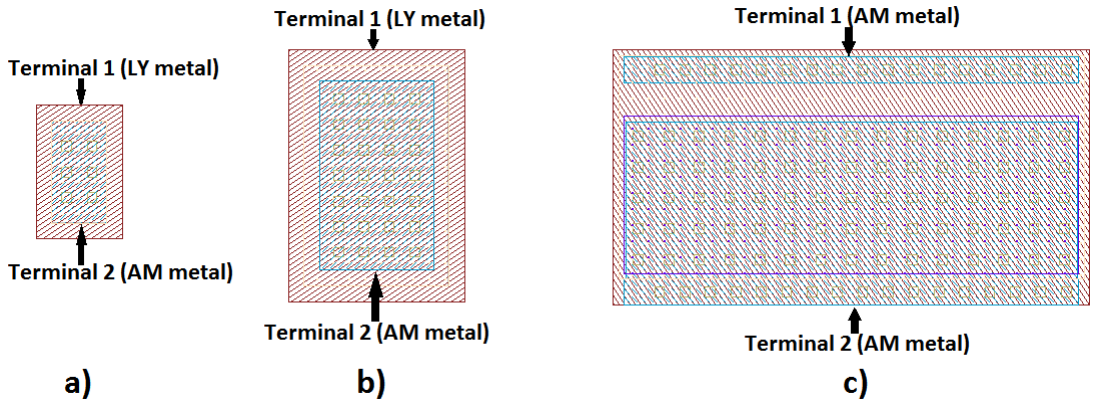

Figure 22 – a) MIM capacitor (93 fF) used for matching purpose. b) MIM capacitor (523 fF) used for AC feed. c) DualMIM capacitor (4.15 pF) used to filter supply noise.

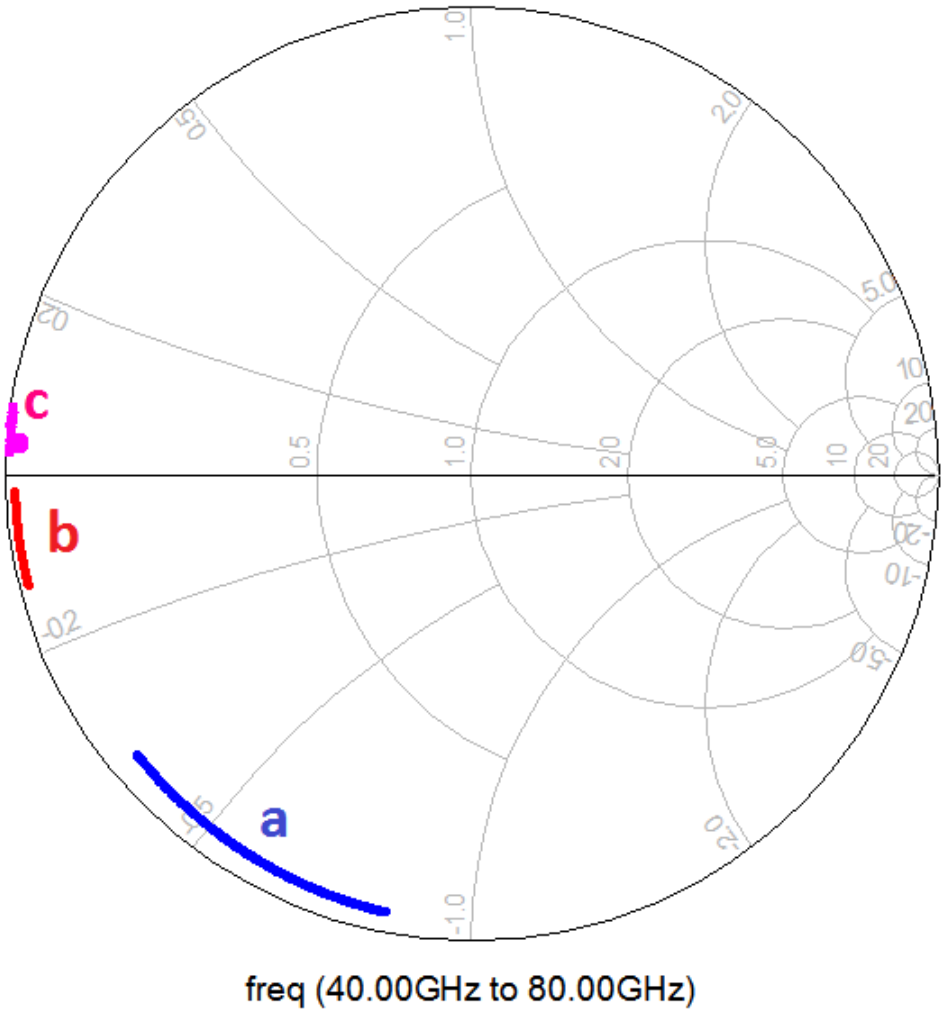

Figure 23 – Behavior of the capacitors of Figure 22 as a function of frequency.

2.4 Transmission lines

The inductors of the design-kit produces inductances that range between 150 fH and 35 nH. At this work we did not use these because, as will be seen further, the needed inductances at 60 GHz for matching purposes are smaller than 100 fH. So, the use of transmission lines (T-lines) are more suitable for synthesize these small inductances. The design-kit has three transmission lines options: rfline, singlewire and singlecpw. The rfline is typically used as an inductive element for applications where low inductance with a high quality factor (Q) is required. It is a line that presents a precise model at high frequency. It is built of AM metal, with no ground plane, and with a length ranging from 100 to 1000 μm, and a width ranging from 4 to 25 μm (Figure 24a). The singlewire is a microstrip transmission line structure that incorporates one or two wires, a metal ground plane, and optional side shields. This transmission line are most appropriate for applications where precise impedance and phase characteristics are desired, such as for routing of RF signals between RF circuit blocks (Figure 24b). It is built of AM and LY metals and has a length that varies between 10 and 180 μm and a width between 2 and 10 μm. The singlecpw is a coplanar waveguide transmission line structure for critical signals where it is not possible to provide defined RF ground planes. It is used in applications such as high speed clocks distribution networks and signal routing in dense analog circuit blocks. It is composed of AM metal and has a length ranging from 10 to 900 μm and a width between 2 and 1000 μm (Figura 24c) (IBM, 2011). For the T-lines with the same length (L = 100 μm) and characteristic impedance (50 Ω), the singlewire and singlecpw lines presents a lower attenuation ($\approx$ 0.077 dB at 60 GHz) compared to rfline ($\approx$ 0.16 dB at 60 GHz). On the other hand, to synthesize a certain inductance with these lines, the rfline line needs a significantly smaller length ($>$ 2x smaller), therefore occupying a smaller area. This is a even more restriction for the singlewire, which has a very limited length, requiring more than one of these in series (consequently more interconnections and losses) to obtain the same inductance of the rfline. The attenuation of these lines as a function of frequency is shown in figure 25.

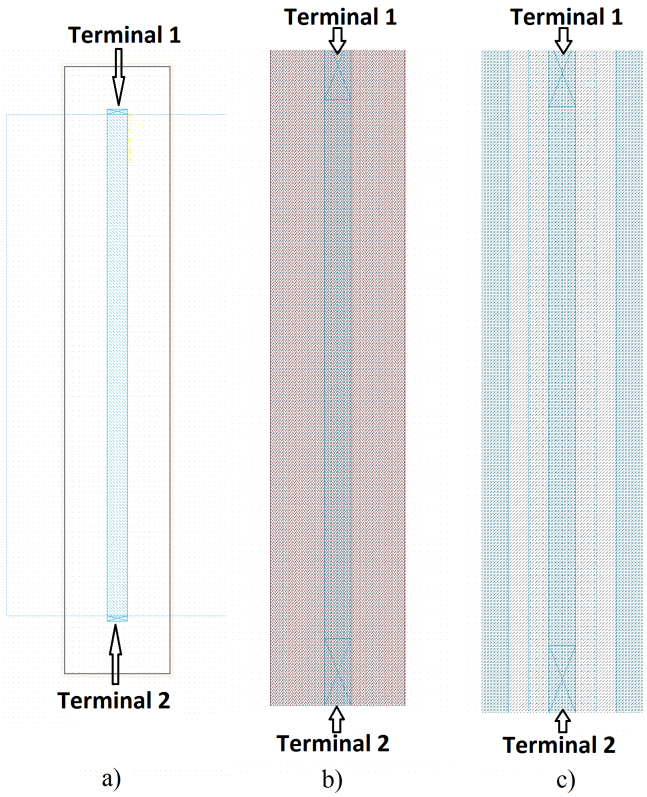

Figure 24 – Transmission lines (Access by AM): a) rfline , b) singlewire and c) singlecpw.

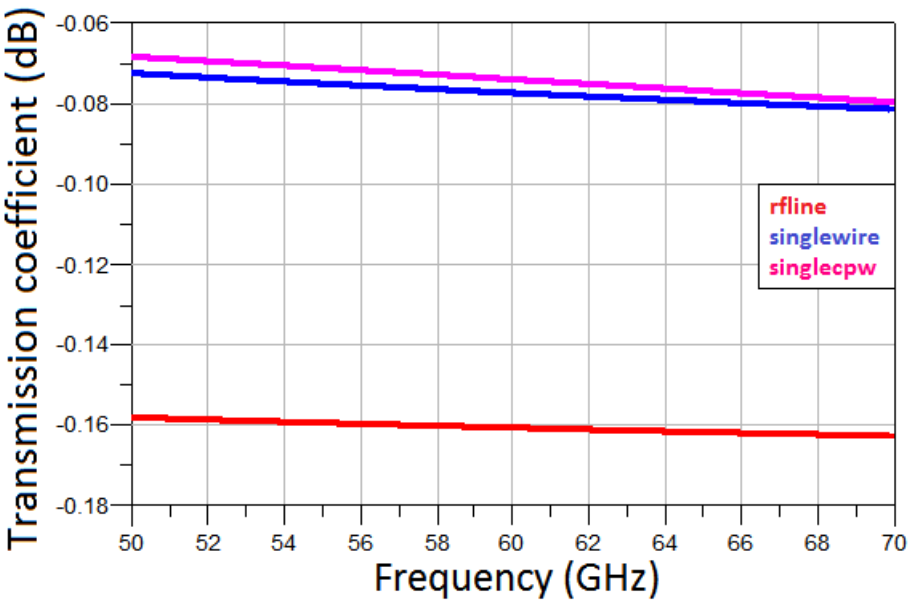

Figure 25 – Transmission coefficient of the transmission lines (L = 100 μm, 50Ω): rfline (red) , singlewire (blue) and singlecpw (pink).

3 Design Procedure

In a amplifier design, whether it is a LNA, PA or other, consists basically of designing three fundamental blocks: an input matching network, an amplification block (active device) and an output matching network, besides the bias circuitry. A simplified diagram of an amplifier is shown in Figure 26. The amplification block consists basically of the active component (transistor) operating in a given class of operation. The input matching network acts transforming the impedance seen by the transistor, seeking to maximize the power transfer between the source and the amplification block. The same can be said for the output matching network, whose function is to transform the impedance seen at the output of the transistor, seeking to maximize the power transfer between the amplification block and the load, thus maximizing the amplifier performance. These matching networks are generally synthesized by the use of passive components. The amplification block can be designed by different topologies. In the case of bipolar transistors as active device, the three most common and used topologies are: common-emitter (CE), common-base (CB) and cascode. Figure 27 presents these topologies.

The common-emitter (CE) topology, in comparison with the others, presents a reasonable gain and generates the smallest Noise Figure (NF) among the topologies. In contrast, this topology is the one that presents the worst reverse isolation (specially in high frequencies), resulting in a greater dependence between input and output, and therefore being more susceptible to instabilities.

The common-base (CB) topology presents much less feedback at high frequencies than the CE, making it more stable and simplifying the input and output matching. However, this topology is the one with the lowest gain, besides presenting a Noise Figure that increases with the frequency (DAS, 2013).

The cascode topology consists of the "union" between a common-base (CB) transistor connected at the output of a common-emitter (CE). This is the most versatile of the three topologies, providing the most stable signal gain over the widest bandwidth with only a slight sacrifice in Noise Figure performance (DAS, 2013). Due to the presence of common-base, feedback between output and input is minimized, that means, it presents a high reverse isolation. The cascode features a better gain than the other two topologies, but requires a higher supply voltage, impacting the energy consumption.

In the design procedure of this work, the amplification block will be first designed, then the bias circuitry will be implemented. Next the output matching network will be synthesized, and finally the input matching network will be synthetized, as can be seen in detail in the following sections.

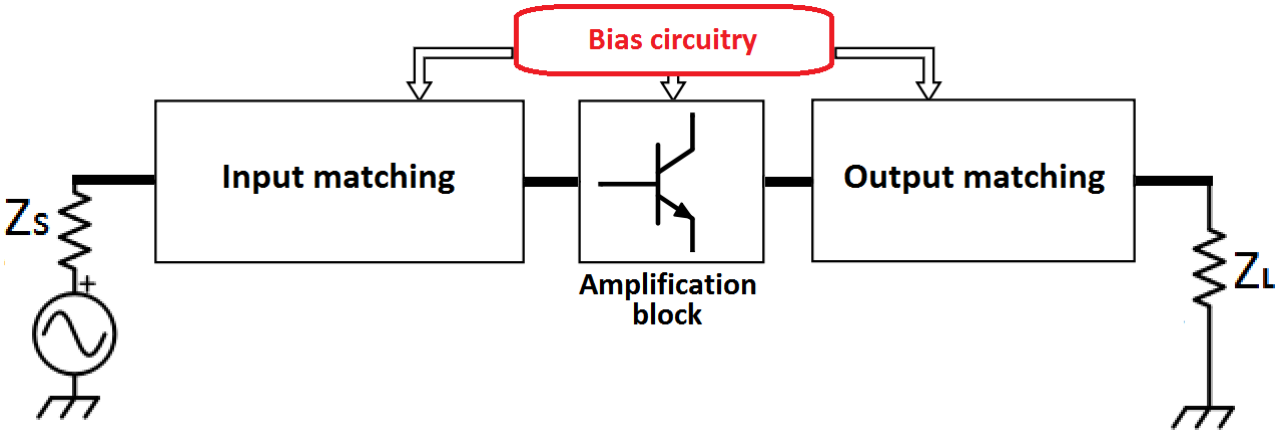

Figure 26 – Simplified block diagram of an amplifier.

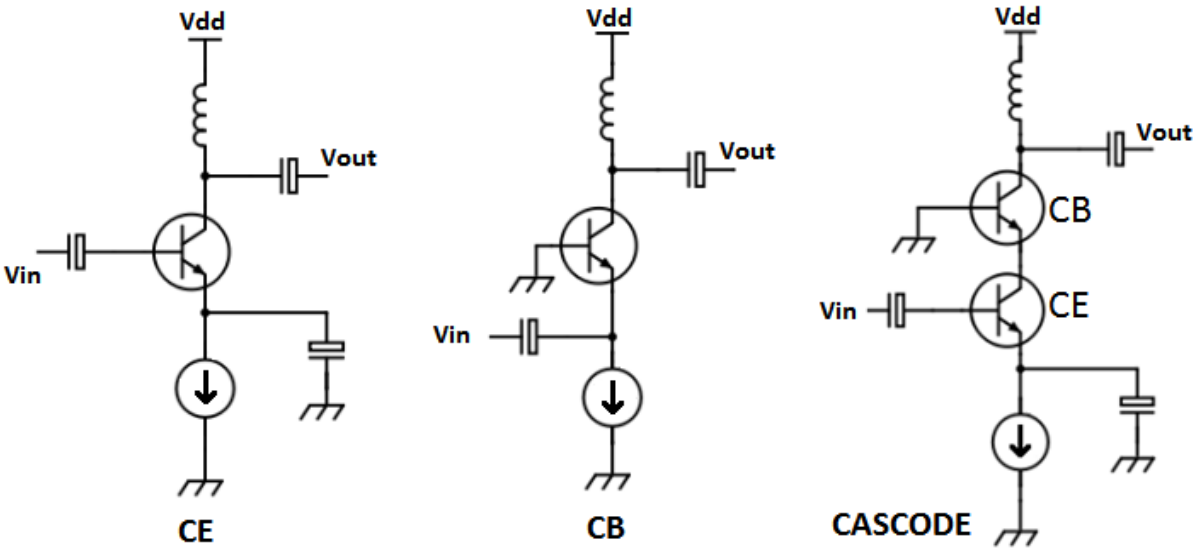

Figure 27 – Amplifier Topologies.

3.1 Choice of amplifier topology

The first step in designing an amplifier is the choice of its topology. As discussed in the previous section, the transistor with higher f_t was chosen automatically because its competitor (with higher breakdown voltage) is not able to operate well in 60 GHz (since its f_t is 57 GHz). Also, this HBT breakdown voltages are $BV_{ceo} \approx 1.8$ V and $BV_{cbo} \approx 5.5$ V. Both breakdown voltages are routinely quoted as figures of merit for bipolar transistors. BV_{cbo} is generally much bigger than BV_{ceo}, due to the DC current gain (β) of the device. So, the use of a common-base topology is preferable instead of a common-emitter, since the first one is limited by a higher breakdown voltage (BV_{cbo}). In (SUN; FISCHER; SCHEYTT,

Parameter	Quantity	Value
P_{sat}	Saturated power	$\approx$ 20 dBm
PAE	Power Added Efficiency	$\approx$ 25%
Gain	Power gain	$\approx$ 10 dB

Table 3 – Target specifications.

2012) it was shown that a common-base transistor can safely operate close to BV_{cbo} if the DC operation is safe. An increased breakdown voltage will allow a larger voltage swing, and consequently an increase in output power. Cascode topology is often used because it has the benefits of a CB and also offers a greater gain and reverse isolation, improving stability. As our output is implemented by a CB configuration, the maximum output voltage swing will be limited to BV_{cbo}. The common-base of the cascode acts as a current buffer for the common-emitter, supporting the majority part of the DC voltage. On the other hand, the common-emitter acts as a transconductance stage and controlls the DC current in the topology. This DC current control is important because, as we will see further, the CB transistor will be taken to a weak avalanche region (with current coming out of the base). Therefore, it ensures the bias of the topology.

To prove the indications that the cascode topology is superior in terms of perfomance, the three topologies were compared (Appendix A). It has been shown that the CE topology is the one with the worst results. The cascode topology was shown to be superior to CB, which was already expected, and therefore was the chosen one to be used at this work.

3.2 Specifications

Reviewing the state of the art (Table 2) in 60 GHz SiGe power amplifiers without power combining techniques (DO et al., 2008; PFEIFFER; GOREN, 2007a; SUN; FISCHER; SCHEYTT, 2012; GRUJIC et al., 2012), one can observe saturated power ranging 15.5 dBm (DO et al., 2008) to 20 dBm (PFEIFFER; GOREN, 2007a), maximum PAE between 12.7 % (PFEIFFER; GOREN, 2007a) and 28.4 % (SUN; FISCHER; SCHEYTT, 2012), and power gain at saturation from 4.5 dB (PFEIFFER; GOREN, 2007a) to 14 dB (DO et al., 2008). This work aimed the design of a 60 GHz power amplifier in SiGe with near 20 dBm saturated output power with the best PAE and power gain values. The target specifications are summarized in Table 3.

3.3 Layout-oriented design

A traditional design is generally comprised in designing the circuit completely in the schematic level. Once achieved the desired results, the layout is designed. In millimeter waves, the impact of the design of the layout may introduce a huge amount of unwanted elements (parasitic elements), which can significantly impact the behavior of the circuit at 60 GHz. At such high frequencies any parasitic elements, however small (e.g. fF capacitances or mΩ resistances), can significantly impact all the behavior of the amplifier by introducing losses and mismatches. To attempt to reduce the large discrepancy (introduced by these parasitics) that could arise if the circuit were completely designed at the schematic level and then passed to the layout, a layout-oriented design approach is proposed. This approach was adopted to decide upon different combinations/arrangements of passive components and interconnections, aiming at reducing the global losses of the PA. This means that the design of the amplifier will be done in stages, and the layout of each stage will be refined multiple times (iterative method) taking into account the post-layout (RC) extraction results. In this sense, the interconnections included in the design-kit of the technology (Tee, Bend, Y junction, etc) will not be used, since these will be implemented and fine-tuned (length, width and shape) aiming the better achievable performance.

In this work we performed post-layout extraction of type RC using Virtuoso ASSURA (from Cadence). This method extract all the parasitics resistances and capacitances of the layers and the coupling between them. However, it is known that at very high frequencies, the most appropriate method to extract all the parasitics elements is by performing electromagnetic simulations. This method is the one that produce results that are more closer to reality (closer to measures) at such high frequencies. In contrast, this method of simulation is much more complex and requires an extremely high computational effort. Also, it is a method that is not found in many of the design softwares (as is the case with Cadence). Due to these factors, coupled with our lack of experience in electromagnetic simulations, we decided to continue using the already well-known parasitic extraction method.

This methodology was divided into four stages. The first one contemplates the design of the PA's core (cascode topology). The second aims the design of the bias circuitry. The third one brings the design of the output matching while the last one aims the design of the input matching. The final layout of each step is fed back into the next step, and so on. A greater emphasis was placed on the loss of the output, but at the end the entire layout was fine-tuned. A simplified block diagram of the design flow is shown in Figure 28. We only pass to the next stage in the design flow when we obtain satisfactory results, that means, when we have a post-layout results as close as possible from the schematic ones. If at the end the layout of the circuit is unstable, a new design must be started including some stability technique, such as an interstage inductor between the CE and the

CB (which will also introduce losses).

3.3.1 PA's core design

Once the cascode topology has been chosen, the next step is the load-pull simulation of this structure. This analysis allows to systematically vary the real and imaginary parts (using a tuner) of the load impedance, so as to trace constant power (or PAE) contours in the Smith chart. The tuner is configured to synthesize a wide range of impedances to be viewed at the output of the transistor, while the source remains as the conjugate complex of the input impedance.

Figure 29 shows a generic setup of a load-pull measurements analysis. The Device Under Test (DUT) is connected between tuners (which will synthesize impedances), and these tuners are connected to bias circuitry. A controller (e.g. PC) manages at the same time the power available by the the signal generator, the power measured at the power meter and the tuners, providing the load-pull measurements.

In our design, a load-pull simulation of the cascode were done, including optimization of bias and transistor geometry parameters. For the bias, parameters such as base voltage (VB) at the common-base, the supply voltage (VDD) and base current of the common-emitter were optimized. On the other hand, emitter length and multiplicity were the optimized geometric parameters. The optimization was carried in Advanced Design System (ADS) by Keysight. This setup can be seen in Figure 30.

This load-pull analysis seeks better results using power delivered and PAE as main goals. In addition to obtaining optimized parameters of bias and geometry, this simulation indicates the optimal value of the output impedance (for large-signal operation) and input impedance, which must be synthesized to produce the expected results (of power, gain and PAE). Several configurations using the setup of Figure 30 were found, but only a few showed a saturated output power above approximately 20 dBm with a gain and PAE within our specifications. These ones have been implemented using the obtained parameters with the addition of input and output ideal matching, just to ensure the load-pull results.

The better configuration showed a saturated output power and a maximum PAE near 20 dBm and 40% respectively. Table 4 presents the optimized parameters obtained for this configuration. The load-pull diagram of this is shown in Figure 31. For this topology it was also performed the optimization using transistors with different sizes (CE different from CB), but the previous one (with same size) showed, in general, better results.

Once the core geometry and bias levels have been defined by the optimization setup, we proceeded on the design the layout of this step. This layout-oriented approach focused at power delivered to the load results, since for a fixed input power and bias, a larger output power will lead a better PAE (Equation 1.3) and transducer gain (Equation

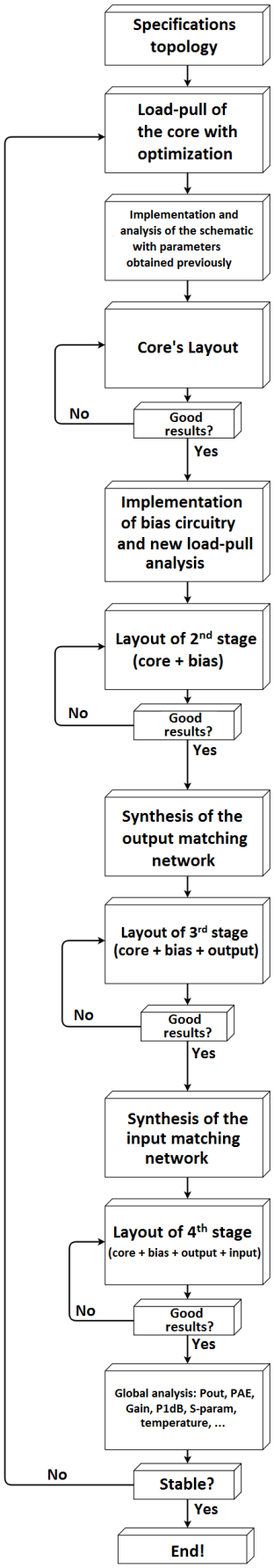

Figure 28 – Design flow block diagram.

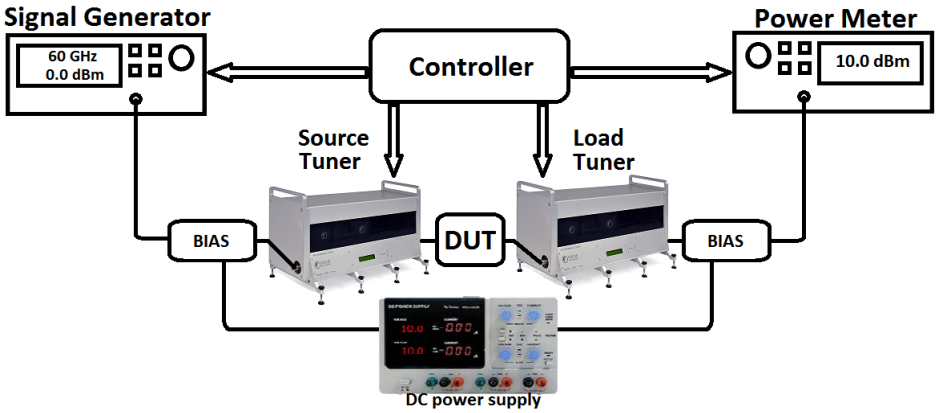

Figure 29 – Generic Setup of a load pull.

Symbol	Quantity	Value
VDD	DC voltage	4.4 V
VB	Base voltage of CB	1.8 V
IB	Base current of CE	270 μA
IC	Collector current	60 mA
exl	Emitter length	4.63 μm
Mult	Multiplicity	11

Table 4 – Optimized parameters.

1.4). Also, we concentrated in the results of power delivered to the load only in the region of large-signal operation (near 5 dBm of input power). This was done in this way to reduce the huge computational time spent in the simulation of the circuit including all parasitics elements. As this approach considers numerous layout iterations in each stage, reducing the time spent on each of these iterations was crucial to the smooth running of the design.

The first core's layout showed the difficulty in interconnecting 11 (see Table 4) common-emitter alongside with 11 common-base to form the cascode configuration, presenting too many losses. Therefore, we opted to change the configuration of the geometry to a similar one, maintaining the total area of the emitter and decreasing the number of transistors in parallel. The total length of the transistor emitter was 50.93 μm (11 x 4.63 μm)(see Table 4), then we first changed to 51 μm (3 x 17 μm). Simulation results showed that 54 μm (3 x 18 μm) presents closest results with respect to the first one (originally planned). The cascode circuit of this configuration is shown in figure 32. The load-pull diagram of this configuration is shown in Figure 33. A maximum power delivered to the load of 20 dBm with a PAE of 36% can be observed. Then we designed the layout of this new configuration. The optimum output and input impedances obtained through load-pull analysis of this configuration were 12.403 + j22.23 (optimal impedance) and 3.245 + j2.71 (complex conjugate of the input) respectively. These impedances were used for matching the core's layout ideally (through an impedance block). Figure 34 compares the power

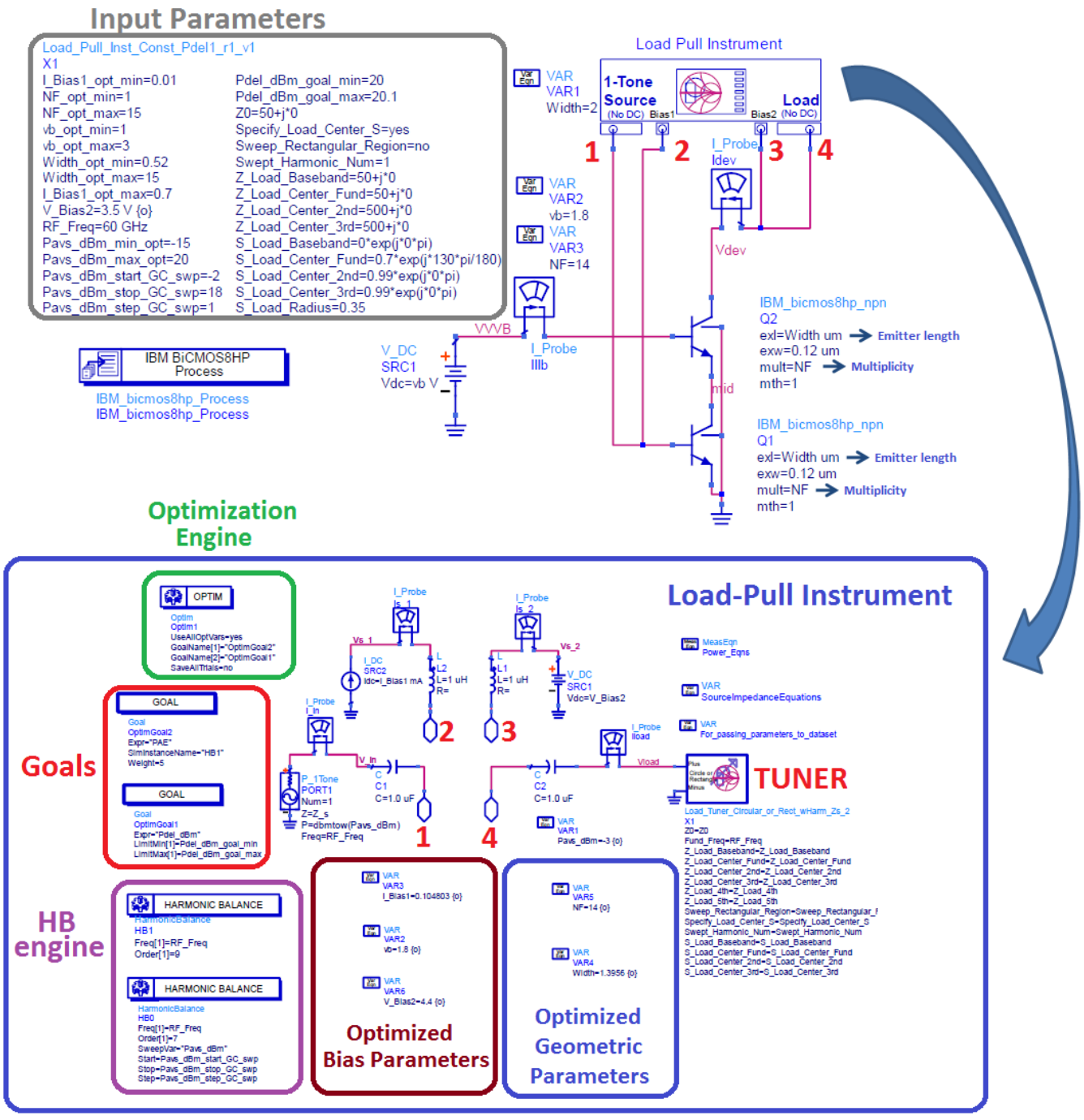

Figure 30 – Our load-pull setup in ADS.

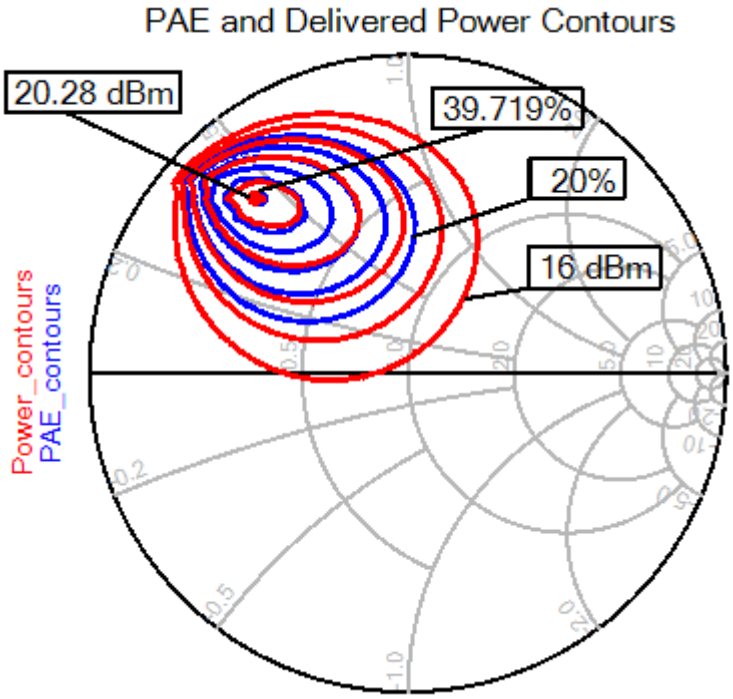

Figure 31 – Load-pull diagram for the cascode configuration with the parameters of table 4. Pavs = 5 dBm and 60 mA of collector current.

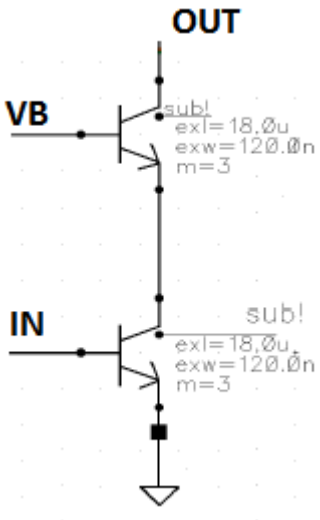

Figure 32 – Cascode circuit.

delivered to the load between the schematic and the first and last layouts.

In this process of transition from the first to the last layout, the transistors were placed as close as possible from each other. The interconnections were made aiming at reducing losses, through decreasing the access resistances of the transistors. In addition, the transistor used has a CBEBC configuration, as already mentioned, with all terminals having access to the metal M1. So to be able to correctly route all the terminals, some of them need to raise a metal level (for M2) through the use of vias, increasing the losses.

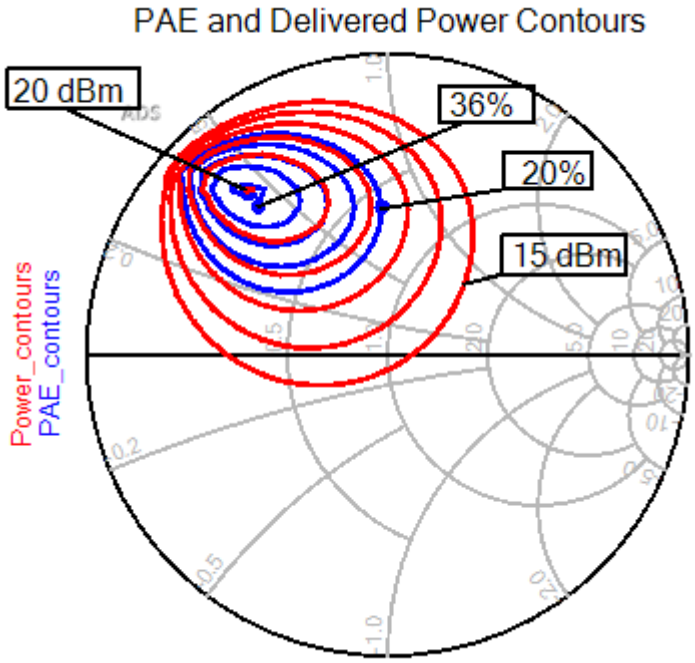

Figure 33 – Load-pull diagram for the cascode configuration with: 1.8 V (VB) , 4.4 V (VDD), exl = 18μm , Mult = 3 , Pavs = 5 dBm and 60 mA of collector current.

The configuration that presented less losses was the one with the base terminal connected to the M2 metal, while the emitter and collector remained with accesses by the M1 metal. Figure 35 shows the final circuit and layout of this step.

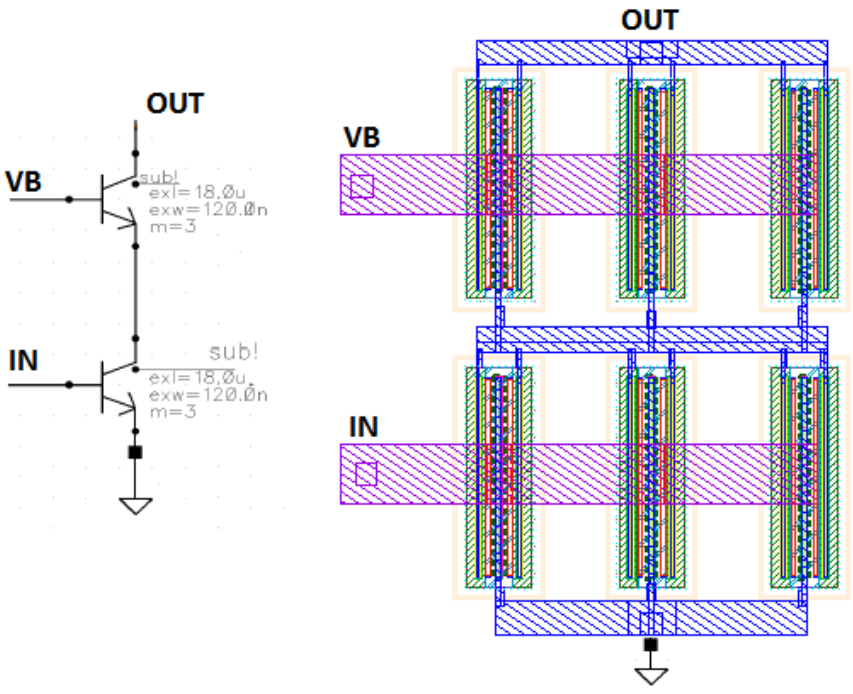

Figure 35 – Core's layout.

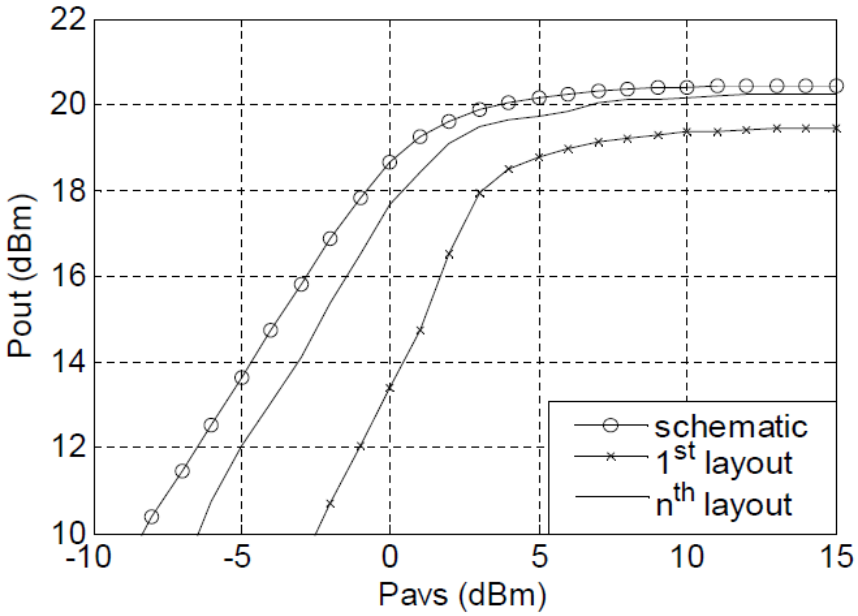

Figure 34 – Power delivered to the load (Pout) at schematic level, first and last layout (1st stage).

3.3.2 Bias circuitry design

The next step of our approach was to design the bias circuitry. The cascode needs 1.8 V at the base of the CB (VB) and approximately 270 μA of base current at the CE yielding an expected collector current around 60 mA. In addition, it is desirable to achieve this with a single supply source, avoiding the need of multiple power supplies and DC probes (during the characterization). The CE's bias was made with the use of a oprrpres resistor (11.37$k\Omega$) in series with a rfline (L = 100μm) for AC block. To bias the common-base one resistor (991Ω) in series with two HBT connected as diodes was used, fixing the voltage at the base of the CB at near 1.8 V. This mantains the voltage at the base of the CB, which otherwise vary significantly if a resistive divider was used, since the current coming out of the base (by avalanche) of this transistor would increase this voltage. Additionally a dual MIM capacitor (4.15 pF) is used to ensure AC ground at this base.

The schematic of the bias circuit is shown in Figure 36a. Then a new load-pull analysis was performed in order to refine the optimum output and input impedances. The new output impedance and complex conjugate of the input impedance values were 10.765 + j19.674 and 3.39 + j2.63 respectively. Next we designed the layout of this bias circuitry with the PA's core designed previously. During the layout design iterations, the capacitor was placed as close as possible to the transistor to yield a better AC ground. The feeding paths, where a high current flows, must ideally be large reducing its parasitic resistance and therefore the voltage drop in it. Also the interconnections of this componentes were made aiming at reducing the global losses of the amplifier. Figure 37 compares the power delivered to the load between schematic and layouts (core + bias) both matched ideally

with the input and output impedances of the last load-pull analysis. The final layout of the second step is shown in Figure 36b.

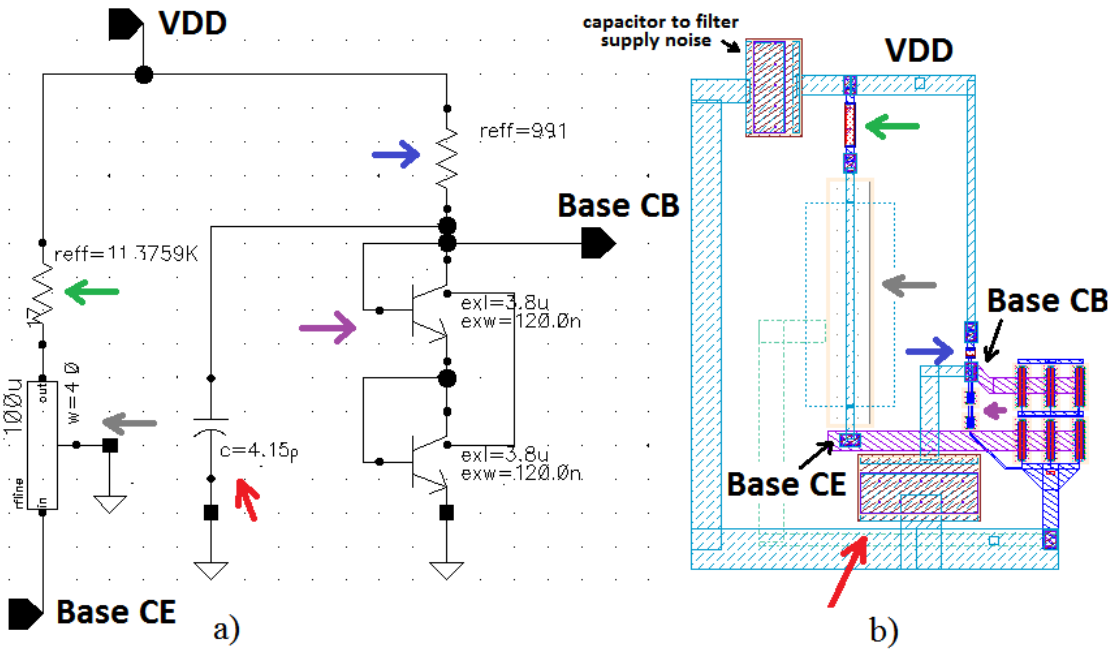

Figure 36 – Schematic of the bias circuit (a) and its layout (b).

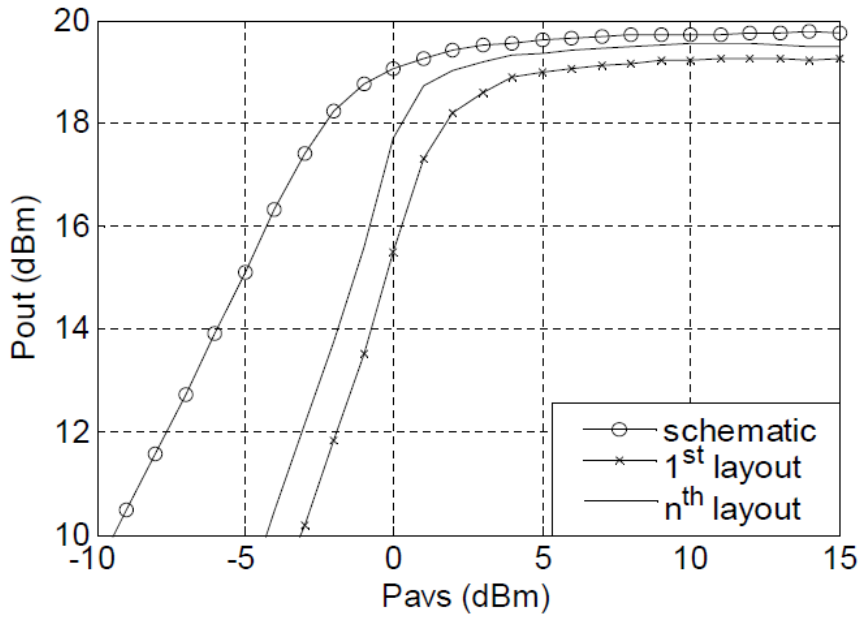

Figure 37 – Power delivered to the load (Pout) at schematic level, first and last layout (2nd stage).

3.3.3 Design of the output matching network

In this step the optimum load impedance (10.765 + j19.674) obtained from the last load-pull analysis was synthesized. First, this impedance is synthesized in the schematic using ideal components (lumped elements). To obtain this impedance with lumped components it was necessary one shunt inductance of 51 pH, one series capacitor of 420 fF (DC block) and one series inductance of 27 pH, besides the pad and the load. Then it is time to replace this lumped components by the real ones of the design-kit of the technology. MIM capacitors and rfline transmission lines were used to synthesize these values. The transmission line chosen was rfline because it is suitable for applications requiring a low inductance with a high quality factor (Q) (IBM, 2011). Corroborating with this indication, during the implementation of amplifiers in preliminary stages of this master's research, the ones whose the matching networks were implemented with this T-line presented better performance in 60 GHz than with the others. MIM capacitors were used because they present less losses for the same capacitance when compared to dualMIM. A fine adjustment (tuning) is necessary to correct the discrepancies that arise from this replacement process (lumped to real). This tuning can be accomplished quickly and easily graphically through the use of the Smith chart in ADS. Output final network includes a MIM capacitor (523 fF) for DC block, two T-lines (rfline) and the output pad (bondpad). Figure 38 shows the impedance, in the Smith chart, seen at the output of the CB transistor (from the CB perspective), as well as the change caused in this impedance by the addition of the components (after correct the discrepancies by tuning). The black dot represents the capacitive impedance seen at the output of the transistor which includes the load, the output pad (major influence), and the DC block capacitor (minor influence). The green and blue (optimal impedance = 10.737 +j19.876) dots represents the impedance seen at the output due the addition of the T-lines as can be seen in Figure 38.

Then the layout of this step was designed, including the previously designed layout (core + bias). During the synthesis of the layout of the output matching network, the input network remained ideal, represented by the complex conjugate impedance of the input (an ideal impedance block). Here in the course of the layout's iterative method, different arrangements of passive components and interconnects between them (size, length and shape) were adopted and tested to choose the one that produced less losses. Figure 40 compares the power delivered to the load between schematic and layouts. The final layout of this part is shown in Figure 39b.

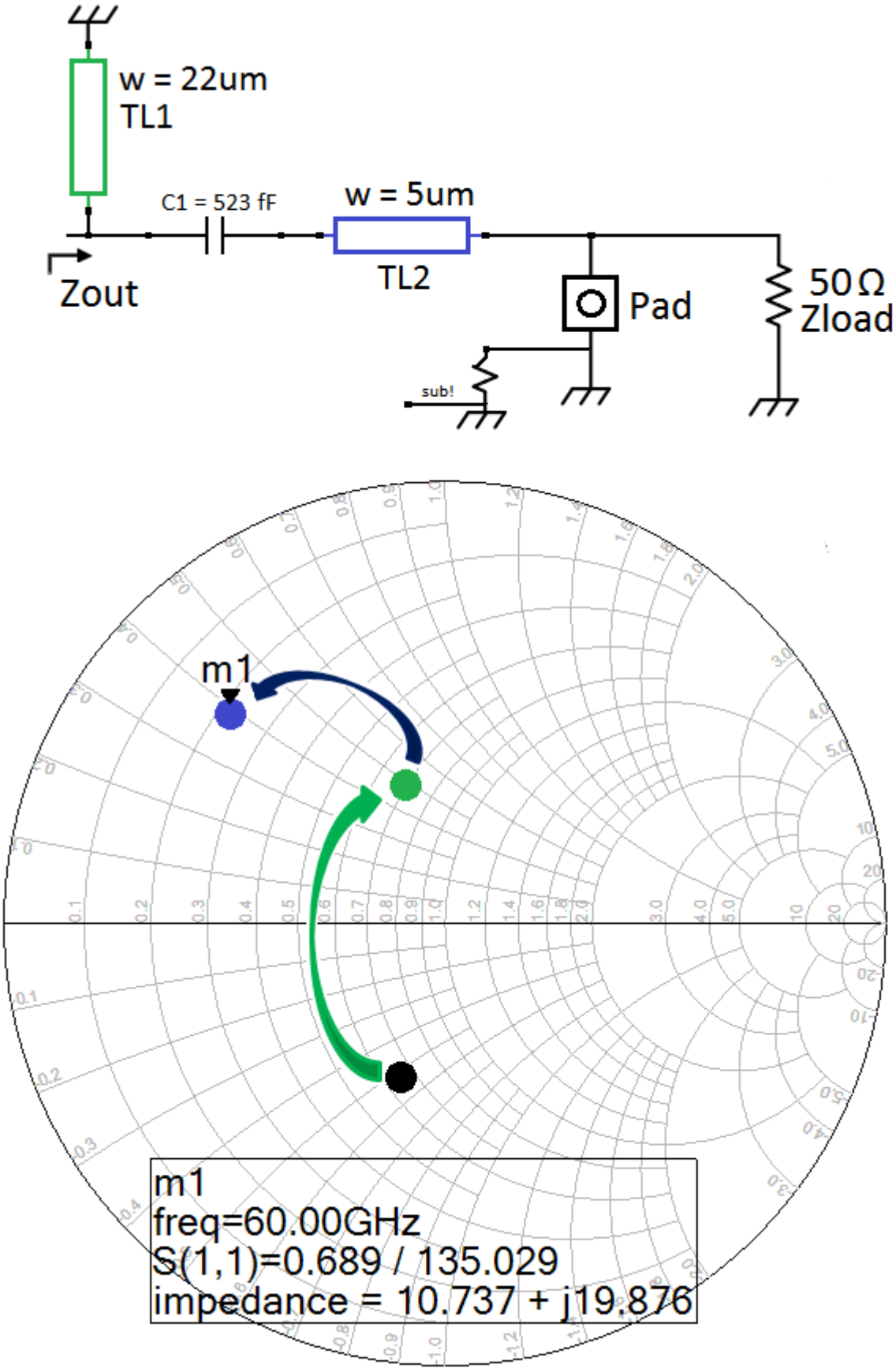

Figure 38 – Synthesis of the output network.

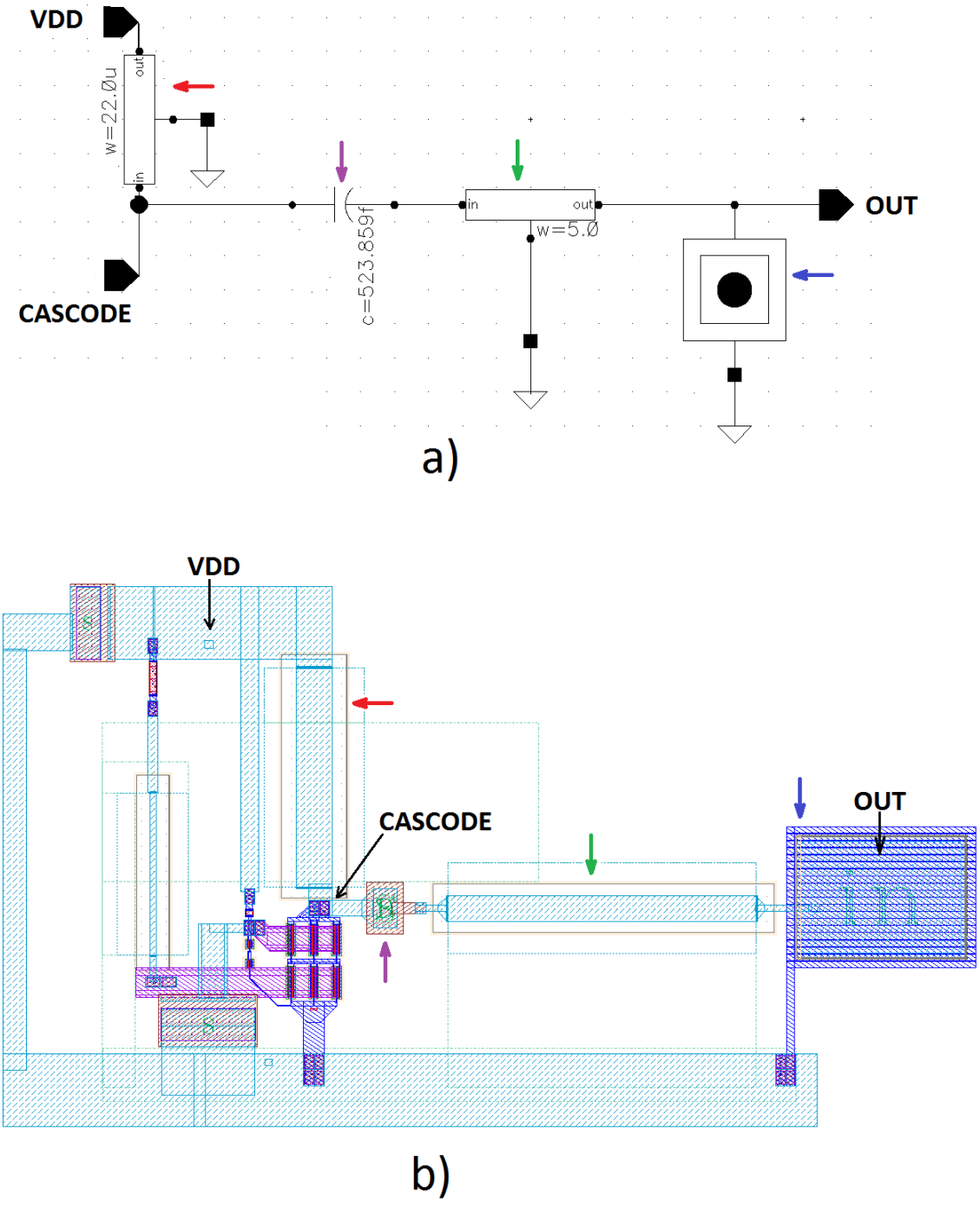

Figure 39 – Circuit of the output matching (a) and its layout (b).

3.3.4 Design of the input matching network

The input matching network is synthesized at this last step by the complex conjugate of the input impedance (3.39 + j2.63) obtained through the last load-pull analysis (in stage 2). In the same way as for the output matching, the input matching network was

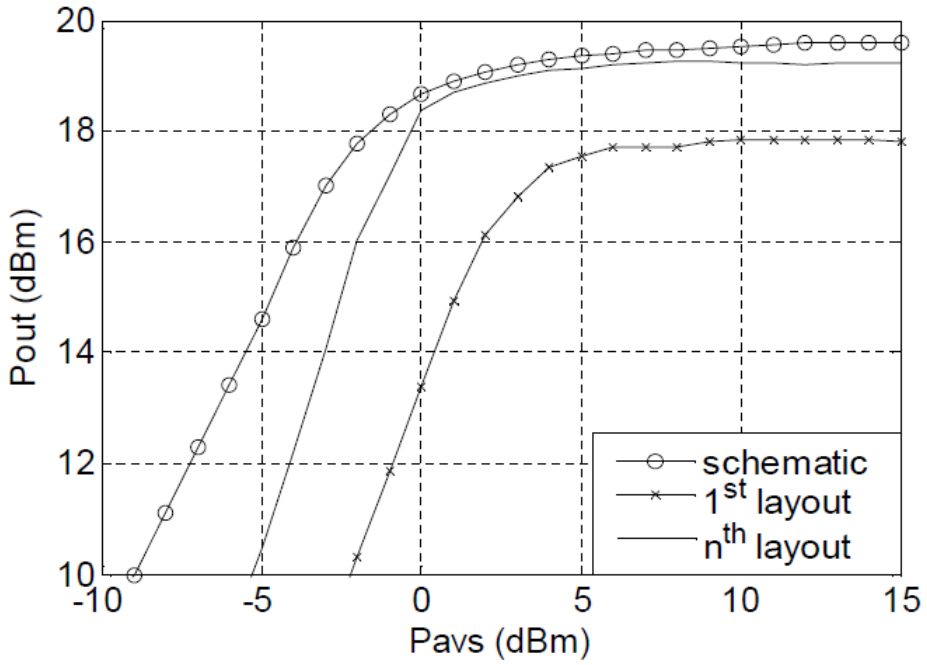

Figure 40 – Power delivered to the load at schematic, first and last layout (3rd stage).

synthesized firstly using ideal components (lumped), and then replaced by the components available in the technology by perfoming tuning with the aid of the Smith chart. To obtain the desired input impedance with lumped components it was necessary one shunt capacitor of 170 fF, one series inductance of 60 pH and one series capacitor of 335 fF, besides the pad and the source impedance. Then it is time to replace this lumped components by the real ones of the design-kit of the technology. MIM capacitors and rfline transmission lines were the real components used to synthesize these values, for the same reasons that was chosen in the last stage. A fine-tuning is then necessary to correct the discrepancies that arise from this replacement process. The input final network includes: input pad (bondpad), one T-line and two MIM capacitors, one of them in series (335 fF) acting as DC block, and the other (243 fF) in parallel for matching purpose. Figure 42 shows the impedance, in the Smith chart, seen from the base of the CE transistor with respect to the source, as well as the change caused in this impedance by the addition of the components (after correct the discrepancies by tuning). The black dot represents the capacitive impedance seen from the base (with respect to the source) of the transistor, which includes the source impedance, the input pad (major influence) and the DC block capacitor (minor influence). The green and blue (optimal impedance = 3.317 +j2.58) dots represents the impedance seen from the base of the transistor due the addition of one T-line and one capacitor, as can be seen in Figure 42.

Once the design has been completed at the schematic level, the layout of the input is implemented from the previous layout (from the previous stage). In this step, the ground pads of the GSG (ground-signal-ground) probes and VDD pad are added. Figure 41

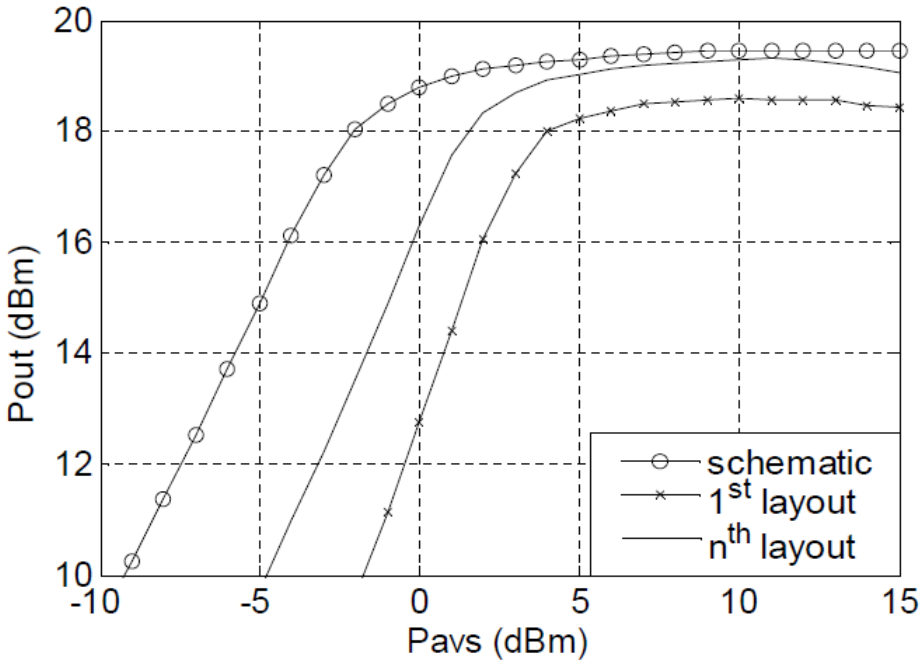

Figure 41 – Power delivered to the load at schematic, first and last layout (4th stage).

compares the power delivered to the load between schematic and the first and last layouts. In the course of transition from the first to the last layout (iterative method), different combinations of passive components and interconnects were adopted and tested to choose the best input matching network, that is, that one which provides less losses between the source and the input of the CE transistor. At the end, the complete layout still does not provide the best possible performance due to mismatches (changes in the input induce mismatches at the output and vice versa). In order to achieve a better performance, the entire layout is fine-tuned. This final fine adjustment allows an increase of about 0.5 dBm of saturated output power. The schematic and final layout of the amplifier as well as the results will be presented and discussed in the next chapter.

At the end of the design, it was attempted to perform electromagnetic simulations of the complete layout using the ADS Momentum Microwave tool. Unfortunately, due to the complexity of the layout, the enormous computational effort required to simulate it did not allow us to accomplish this task (we used a PC with 32 GB of RAM).

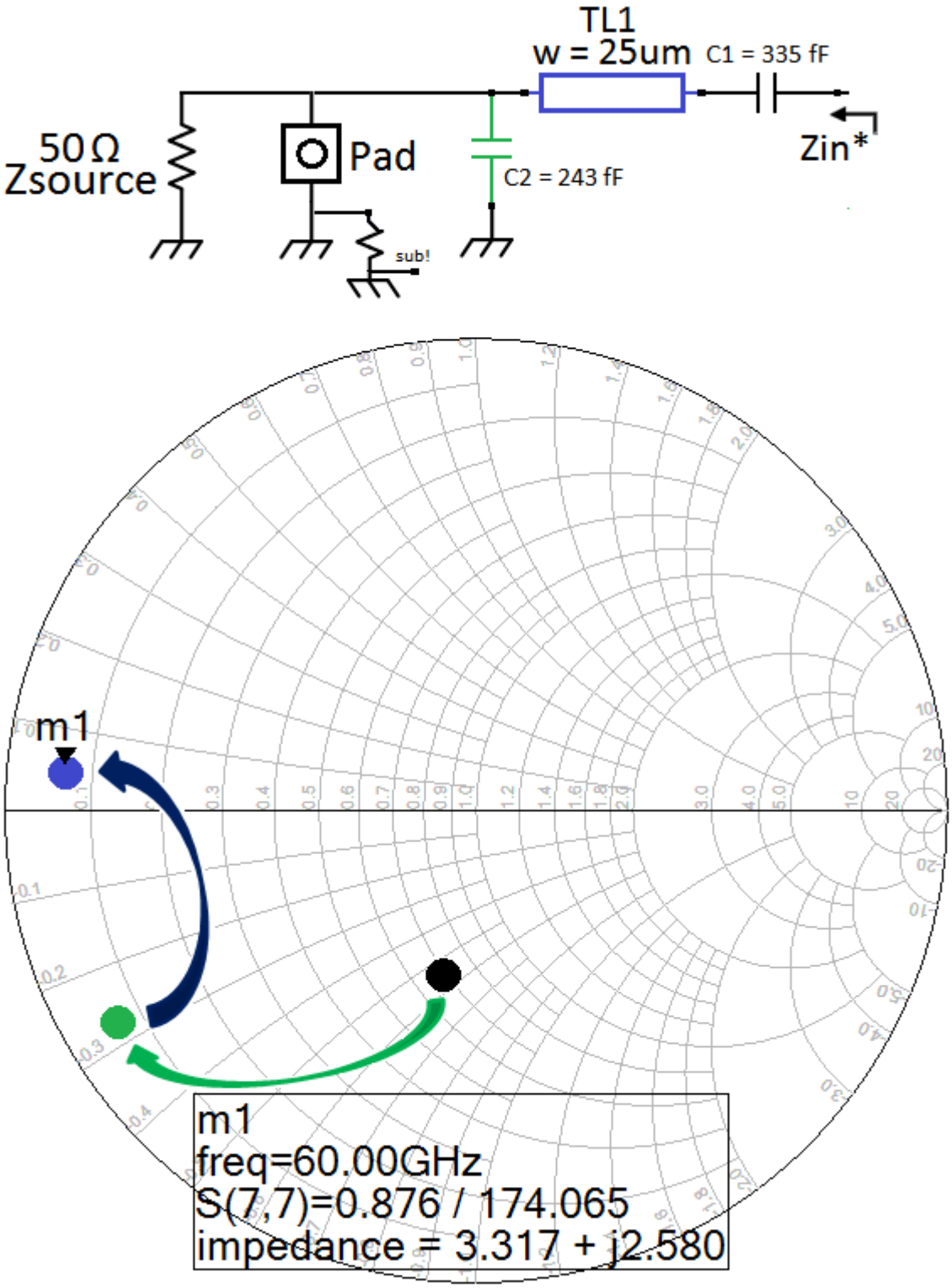

Figure 42 – Synthesis of the input network.

4 Results

In this chapter, we present and discuss the key performance parameters results obtained of the designed power amplifier, in addition to presenting its final circuit and layout. The S-parameters, load-line, stability, temperature and linearity analysis are also discussed. After we compare the results with the state of the art works. At the end, we present and discuss the taped-out chip.

4.1 Power amplifier circuit and layout

The final circuit of the power amplifier, after all steps in the previous chapter have been completed, is shown in Figure 43. The power amplifier final layout occupies an area of 0.95 x 0.5 mm^2 including pads as shown in Figure 44.

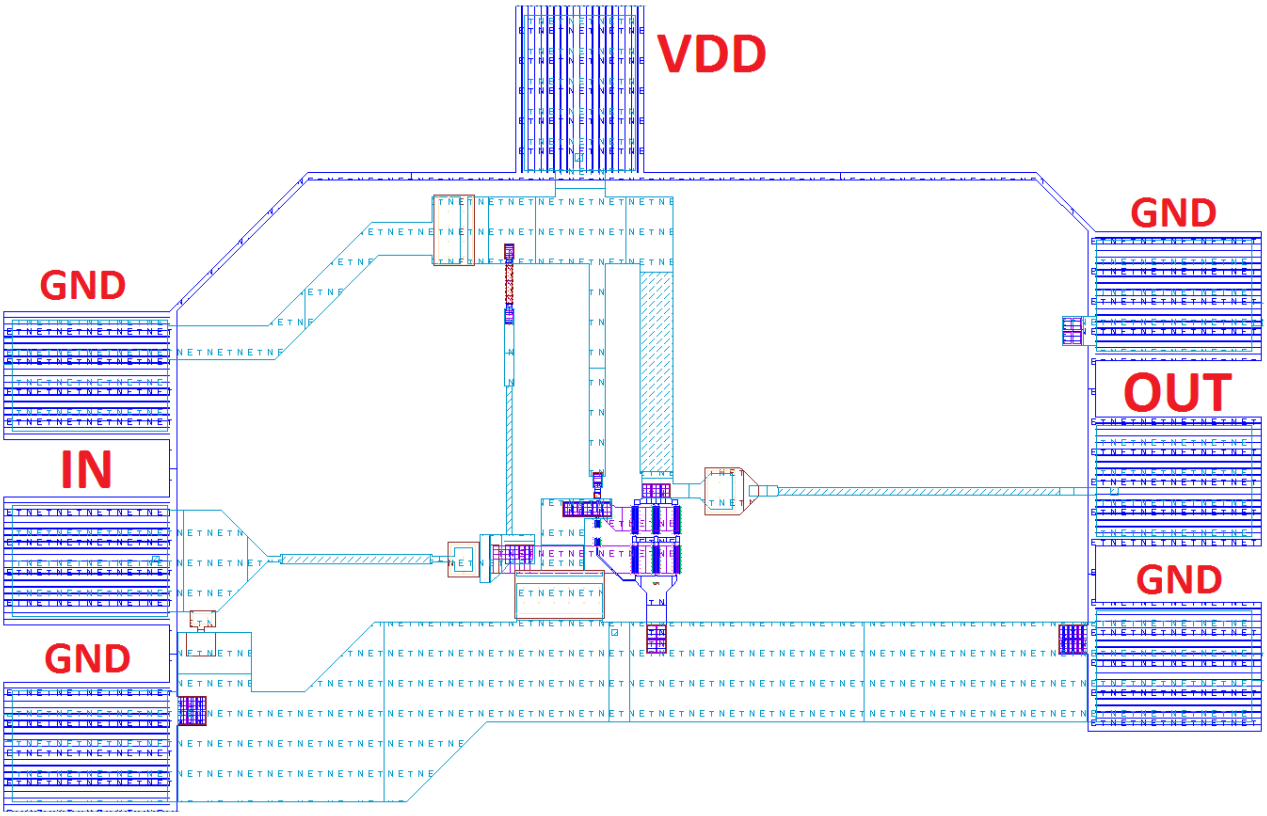

Figure 44 – Final layout of the power amplifier.

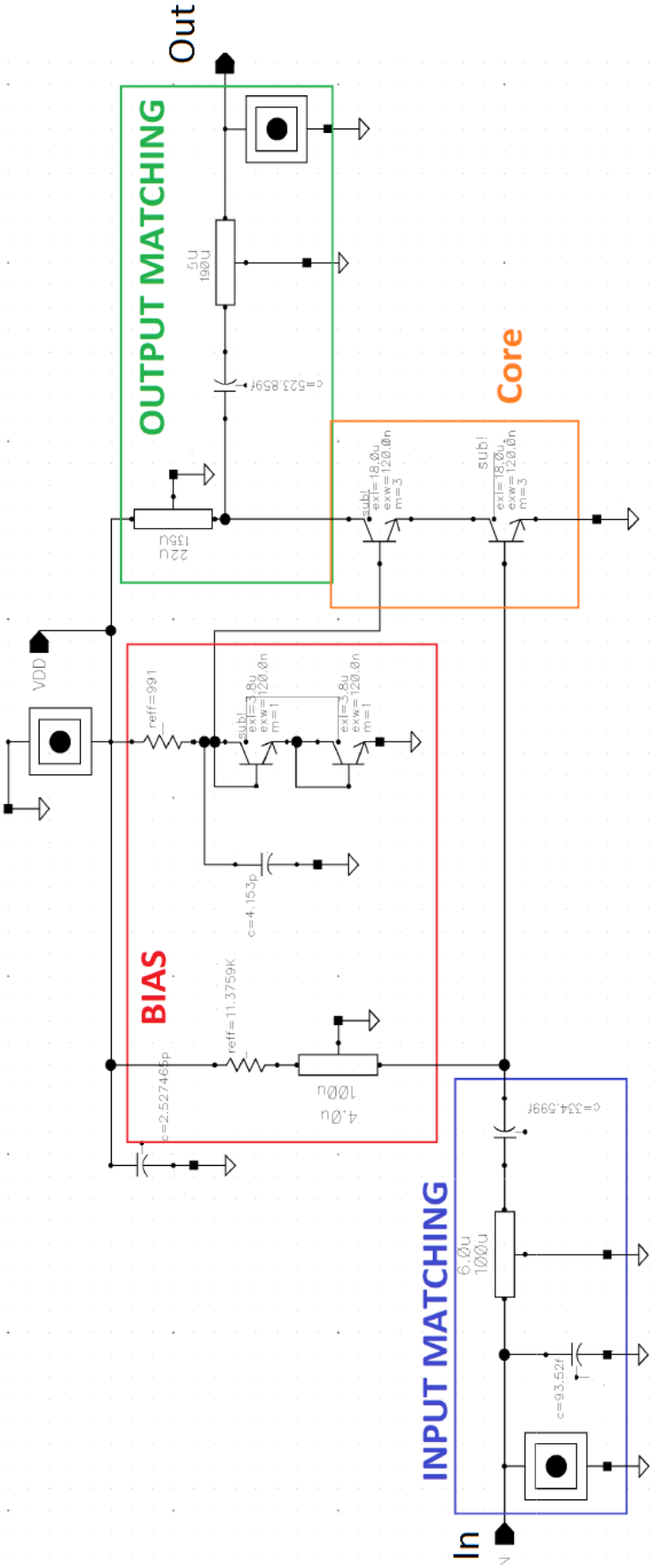

Figure 43 – Power amplifier circuit.

4.2 Power amplifier key performance parameters

The results of power delivered to the load (P_{out}), PAE and transducer gain are shown in Figure 45. Post-layout results show a saturated output power of 19.32 dBm, a maximum PAE of 27.8 % with 10.4 dB of transducer gain at 60 GHz.

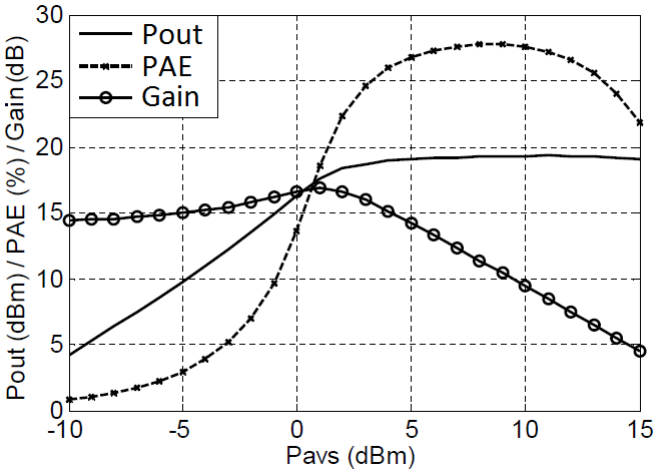

Figure 45 – Power delivered to the load (Pout), PAE and power gain after parasites extraction.

4.2.1 S-parameters

The classical S-parameters analysis considers just small-signal operations. However, there is a more complex and rigorous S-parameters analysis that takes into account the non-linearities of the input signal. It is called as Large Signal S-Parameters (LSSP) analysis. Figure 46 shows the S-parameters of this analysis in a vast frequency range.

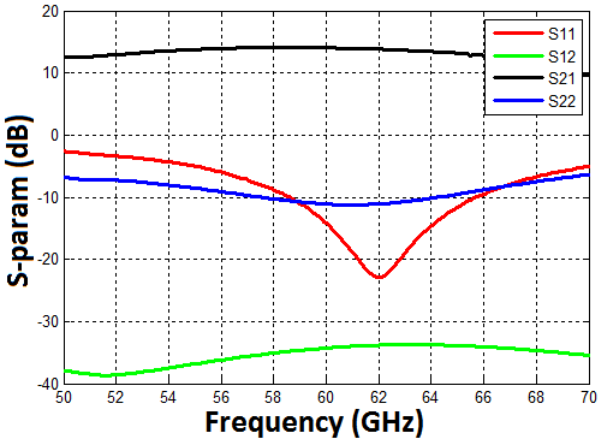

Figure 46 – S-parameters of the amplifier by a LSSP analysis with 5 dBm of input power.

The S-parameters results show input and output matching at the entire unlicensed 60 GHz band (with S11 and S22 < -10 dB), also presenting almost flat gain (S21) above 10 dB. The reverse isolation (S12) remains below -33 dB in the entire spectrum simulated.

4.3 Complementary parameters

4.3.1 Load-line analysis

Figure 47 shows the dynamic load-line of the cascode with 5 dBm of input power. As base voltage of CB transistor is fixed at 1.8 V, the maximum permissible voltage in the collector of this transistor (BV_{cbo}), according to (SUN; FISCHER; SCHEYTT, 2012), will be approximately 7.3 V (BV_{cbo}= 5.5 V + 1.8 V). Under this condition the amplifier will be operating in a weak avalanche region. In Figure 47 the dynamic load line is approaching BV_{cbo}, but does not exceed, indicating that any further collector voltage increase will possible cause collector-base breakdown.

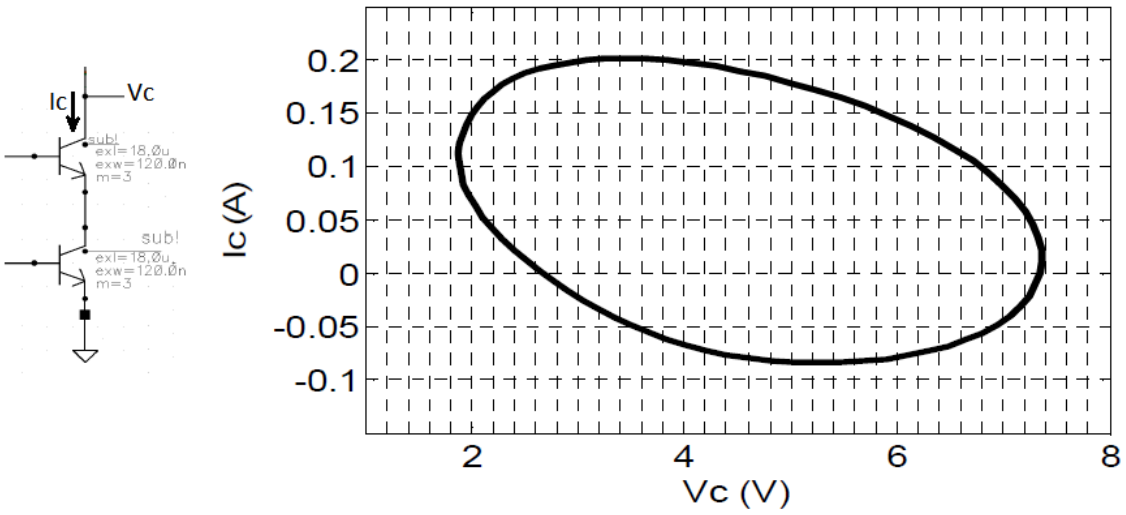

Figure 47 – Dynamic load-line of the cascode.

4.3.2 Stability analysis

Stability is analyzed in Figure 48 by showing Rollet's stability factor (K and $\triangle$), the alternative stability factor (B1) and the stability parameter μ. It shows that K remains greater than unity, $|\Delta|$ smaller than the unity, B1 remains greater than zero and μ greater than unity for a spectrum between DC and 2fc (120 GHz), indicating unconditional stability.

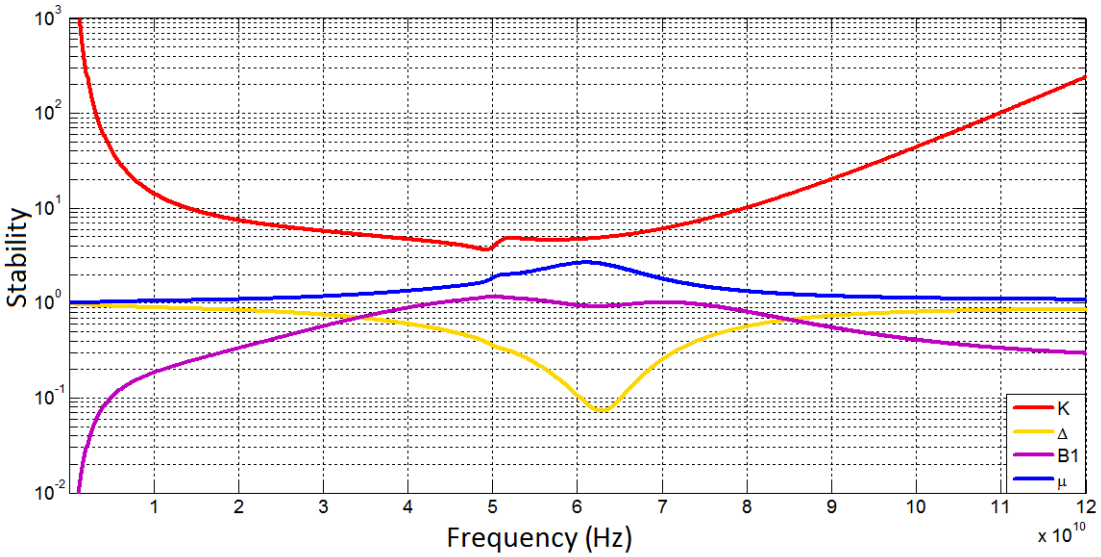

Figure 48 – Stability criteria.

However, these simulations ensures that the PA is stable under stationary condition (small-signal, only fed). We did not performed large-signal stability analysis.

4.3.3 Temperature

The temperature of the common-emitter and common-base were also checked, remaining below 28° C and 110° C respectively in small-signal operations (worst case). This temperature of 110° C is acceptable for power amplifiers operating at small-signal, which is not his standard operation mode. In large-signal operation this temperature drops considerably.

4.3.4 Linearity

In order to evaluate the linearity, the 1 dB compression point (P_{1dB}) was performed. As described in Chapter 2, this parameter can be obtained graphically by extrapolating from the fundamental curve. Here, for a more accurate result, we performed the simulation of this parameter using Cadence. Figure 49 shows the result of the 1 dB compression point (input and output) simulation. We obtained an output 1 dB compression point (OP_{1dB}) of 19.1 dBm and an input 1 dB compression point (IP_{1dB}) of 5.89 dBm.

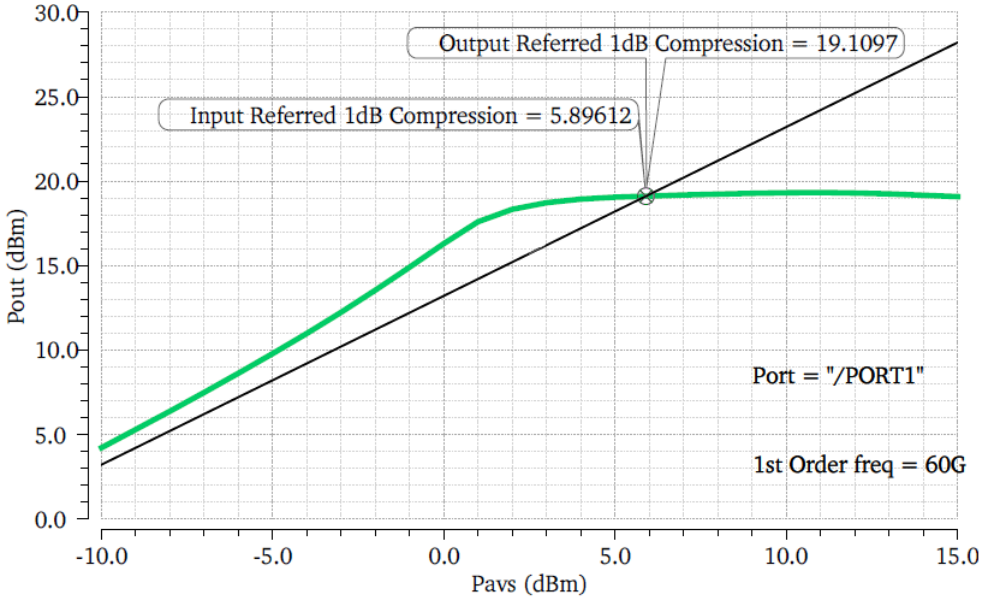

Figure 49 – 1 dB compression point referred to the input and output.

4.4 Comparison with the state of the art

For comparison purpose we summarize the state of the art in 60 GHz SiGe power amplifier without power combining techniques in Table 5. We made this restriction in relation to Table 2 in order to compare the results of similar topologies. Our post-layout results show a PAE very close to the best reported in [6]. The saturated output power and FoM are near to the maximum reported in [1]. Moreover, we used a smaller area, being only greater than that reported in [6].

Ref	[1]	[3]	[6]	[7]	This work
Tec. (μm)	SiGe 0.13	SiGe 0.25	SiGe 0.13	SiGe 0.25	SiGe 0.13
Freq (GHz)	60	61	60	61.5	60
Topology / Architecture	*Push-pull* differential 1 stage	Cascode *single-ended* 2 stages	Cascode single-ended 1 stage	Cascode differential 1 stage	Cascode *single-ended* 1 stage
P_{sat}(dBm)	20	15.5	16.8	17.4	19.32**
$Gain_{sat}$(dB)	4.5	14*	11.4	7	10.4**
$Gain_{max}$(dB)	18	18.8	14.5*	14.2	14**
OP1dB (dBm)	13.1	14.5	11.7	12.2	19.1**
PAE (%)	12.7	19.7	28.4	16.3	27.8**
FoM	84.60	82.95	81.39	79.49	83.20**
Supply (V)	4	3.3	4	3.3	4.4
Pdc (mW)	248	132	64	257.4	277.2
Area (mm^2)	0.975	0.795	0.2	0.62	0.475

*estimated from the plots **post-layout results
[1](PFEIFFER; GOREN, 2007a);
[3](DO et al., 2008);
[6](SUN; FISCHER; SCHEYTT, 2012);
[7](GRUJIC et al., 2012);

Table 5 – Comparison with the state of the art.

4.5 Tape-out

Unlike CMOS technology, SiGe ones requires more effort to be fabricated by MOSIS (MOSIS, 2018), that is, this is a more restrictive technology. MOSIS has an educational research program that allows the fabrication (for free) of chips for research groups. Because a SiGe-based process is more expensive than a CMOS one, there are some restrictions for it to be accepted for manufacture. In order to be able to tape-out our PA in this technology, we needed to write a project about it to be evaluated by MOSIS. This project contained a detailed description of our amplifier including all results obtained by simulation. It was also necessary to describe in detail the routine that would be taken for the measurements of the circuit. The project was evaluated and accepted by MOSIS, which provided us a total chip area of 1 mm^2 in this technology. Next we had to add our PA to the chip that would be sent to the manufacturing. In this step, there are additional Design Rules Check (DRC) simulations that must be done to ensure the integrity of the chip, and to ensure that it complies with all the foundry's manufacturing rules. In this sense, one must guarantee the required levels of local and global densities of all metals layers.

The power amplifier was part of a tape-out in late 2017 by MOSIS. This was the

first SiGe-based circuit shipped to manufacture by RFWild's laboratory. To the best of our knowledge, it is also the first SiGe-based circuit to be completely designed (and shipped to fabrication) in the northeast of Brazil. Figure 50 shows the chip sent to the manufacturing, containing the power amplifier (at the top) and a push-push oscillator (60/120 GHz), also designed by our research group of RFWild's laboratory. Figure 51 shows the chip received in late May 2018. The first experimental measurements took place in August and the results are presented in the next subsection.

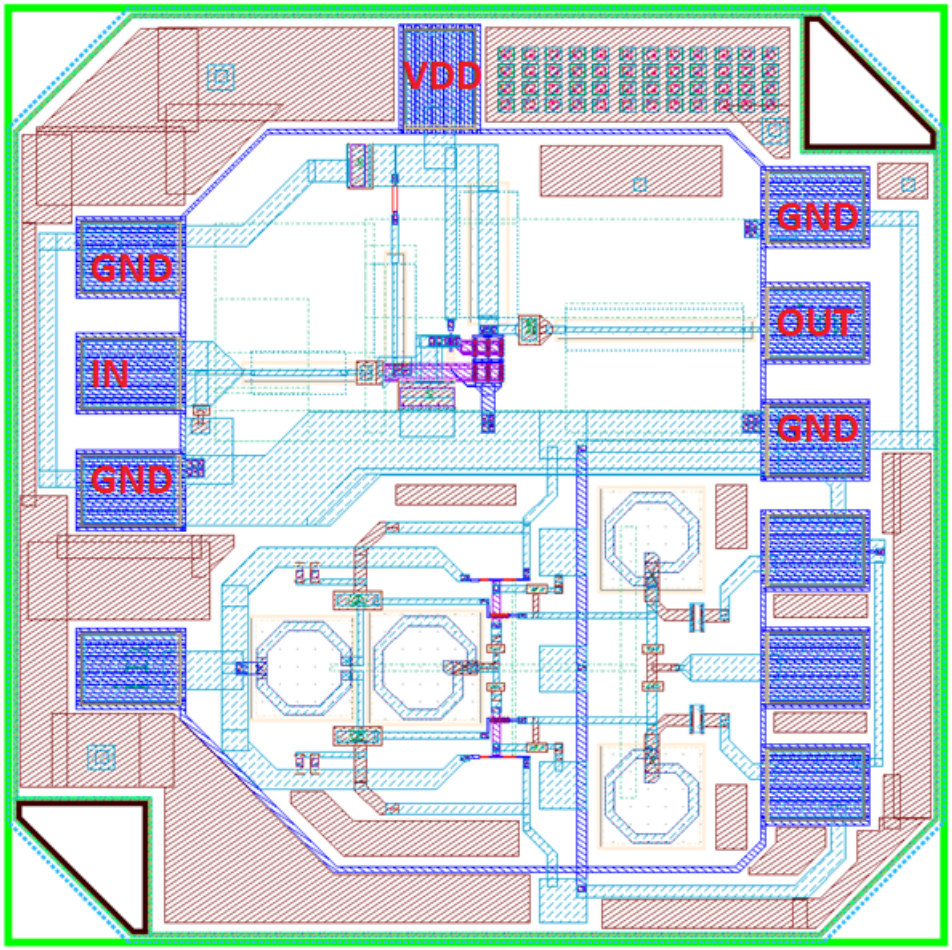

Figure 50 – Chip with a die area of 1 mm^2.

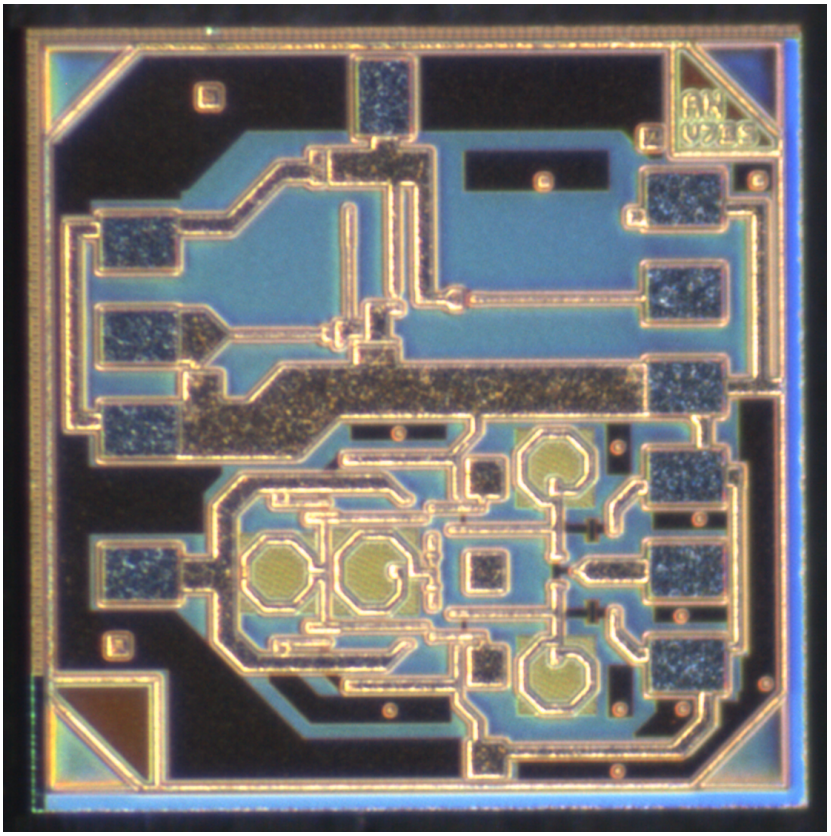

Figure 51 – Microphotography of the chip of Figure 50.

4.6 Experimental results

For the characterization of the circuit, we used the measurement infrastructure of the IMEP-LAHC (Grenoble-INP) laboratory shown in Figure 52. The first experimental measurements were performed using a setup with an Anritsu model 37397D (up to 65 GHz) VNA (Vector Network Analyzer) to analyze the S-parameters of the network. We used GSG probes on the input and output, and a GS probe for DC biasing the circuit. Initial measurements with this setup indicated an unstable behavior for lower than nominal supply voltages. So, we focused first on analyzing this unstable behavior. The S-parameters results of two samples of the circuit using this setup are shown in Figure 53. It can be observed unstable behavior near 30 GHz, where S11 and S22 $>$ 0 dB. It can also be observed that there is no gain (S21) above 38 GHz. Then we implemented the same setup with the addition of a substrate of alumina below the circuits avoiding metallic contact of the chuck with the IC substrate. Also the GS probe was replaced by a DC one. Figure 54 shows the S-parameters for two other samples of the circuit using this second setup. Again an unstable behavior near 30 GHz was observed where S11 and S22 $>$ 0 dB. We did not performed S-parameters measurements with the nominal supply voltage because, as we will see forward, the circuit burns near 4 V.

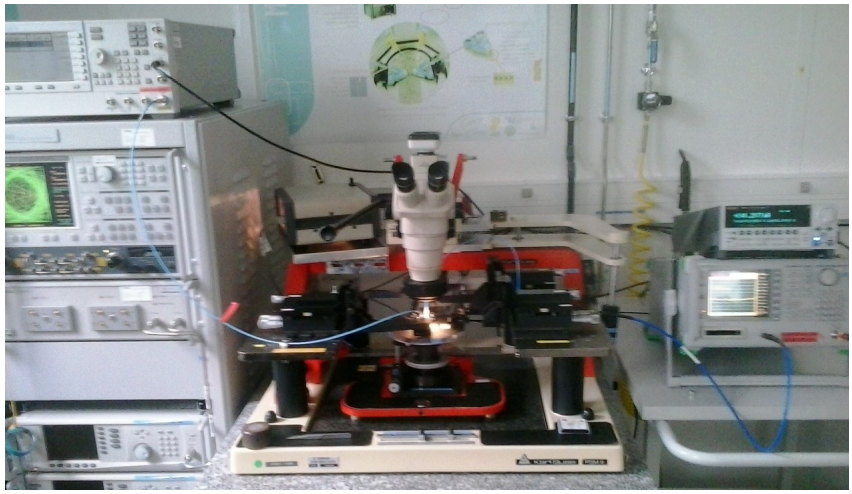

Figure 52 – Measurement bench used for characterizing our chips (IMEP-LAHC).

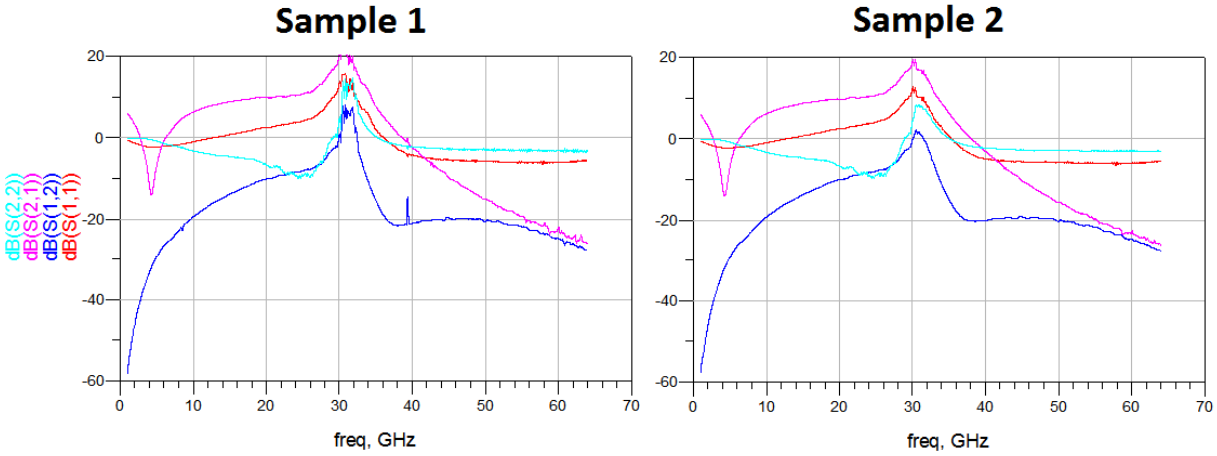

Figure 53 – S-parameters results for two samples of the circuit with supply voltage lower than nominal (VDD = 3.5 V).

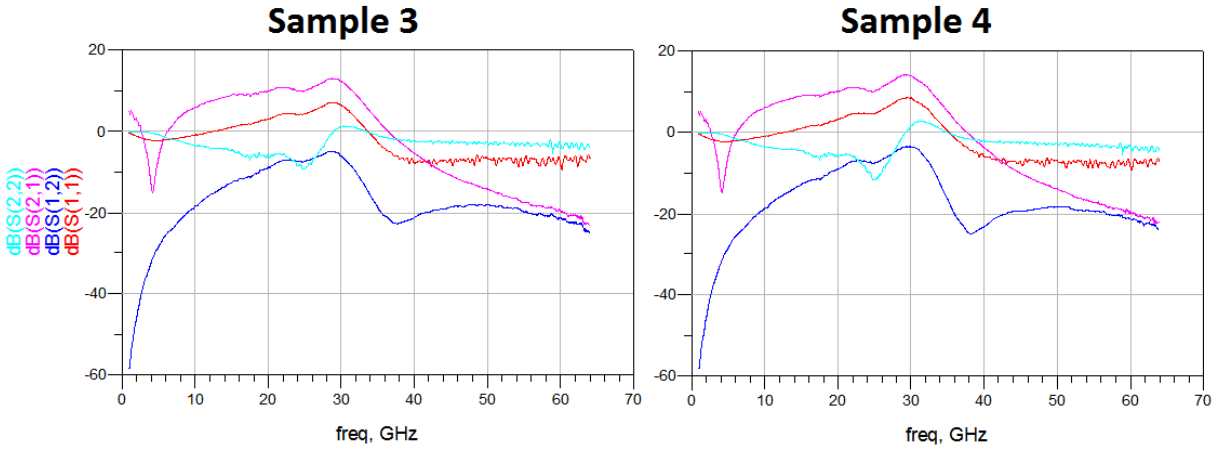

Figure 54 – S-parameters results for two samples of the circuit with supply voltage lower than nominal (VDD = 3.7 V), and with the addition of a substrate of alumina.

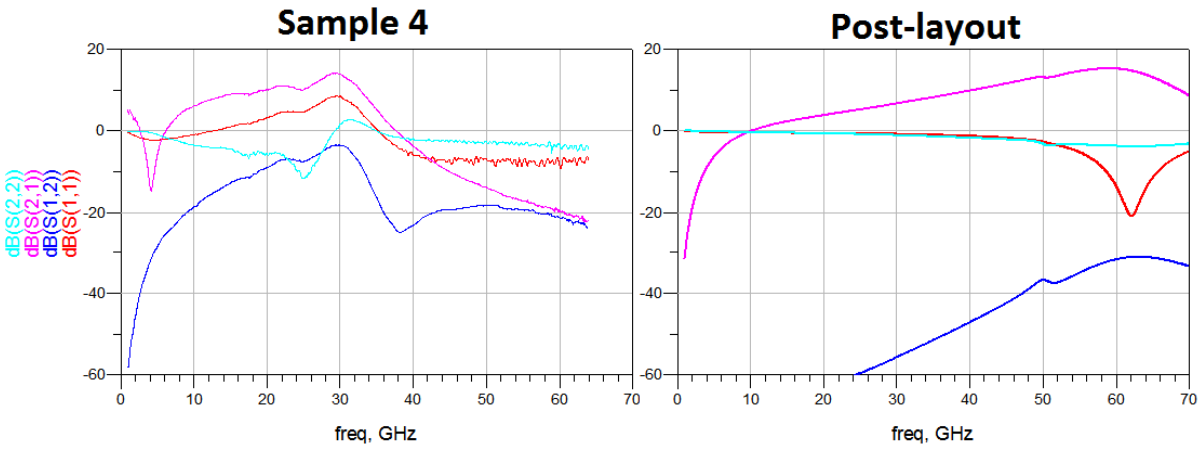

Figure 55 – S-parameters results of the sample 4 (VDD = 3.7 V) and post-layout (VDD = 3.7 V)

Figure 55 compares the S-parameter measurements of sample 4 and the post-layout results, both with 3.7 V of supply voltage. As can be seen, the results are completely different. One of the possibilities for this large discrepancy was the use of RC-type extraction, which is not the best suited for very high frequencies. It is also important to mention that the results of post-layout S-parameters with this supply voltage (3.7 V) are very close to the results with the nominal supply voltage (Figure 46). A greater discrepancy occurs in the comparison of S22 parameter, which no longer has a value of -10 dB in the unlicensed band. With the supply voltage of 3.7 V, this parameter presents in simulation a value of around -3.5 dB, indicating an output mismatch.

In order to try to verify by simulations these instabilities observed with this setup, the stability analysis of the final layout was redone for lower than nominal supply voltages, i.e., lower than 4.4 V. These simulations were not thought a priori since in the literature the stability analysis is commonly performed for only the operating conditions of the circuit. Figure 56 shows the stability analysis (K and B1 parameters) for a supply voltage between 1 and 4 V. As can be seen in Figure 56, for supply voltages lower than 3.8 V the circuit becomes potentially unstable (with $K < 1$ and/or $B1 < 0$). However, the frequency range of possible instability goes from around 55 to 65 GHz, a much different range from that of the instabilities experimentally observed (near 30 GHz). Again, this points to a lack of accuracy of our parasitic extraction method (RC only). We went further and simulated the PA with supply voltages of 3.7, 3.5 and 3.0 V using harmonic balance set as oscillator type, but no oscillations were found with these simulations.

Then we came back to measurements and implemented another setup including a signal generator (model E8257D) at the PA input and a spectrum analyzer at its output (model MS2668C). This setup was implemented with the goal of characterizing the PA with a setup closer to that used for unstable circuits (e.g., oscillator), in order to ensure the instabilities observed with the previous setup. We continued using GSG probes at the

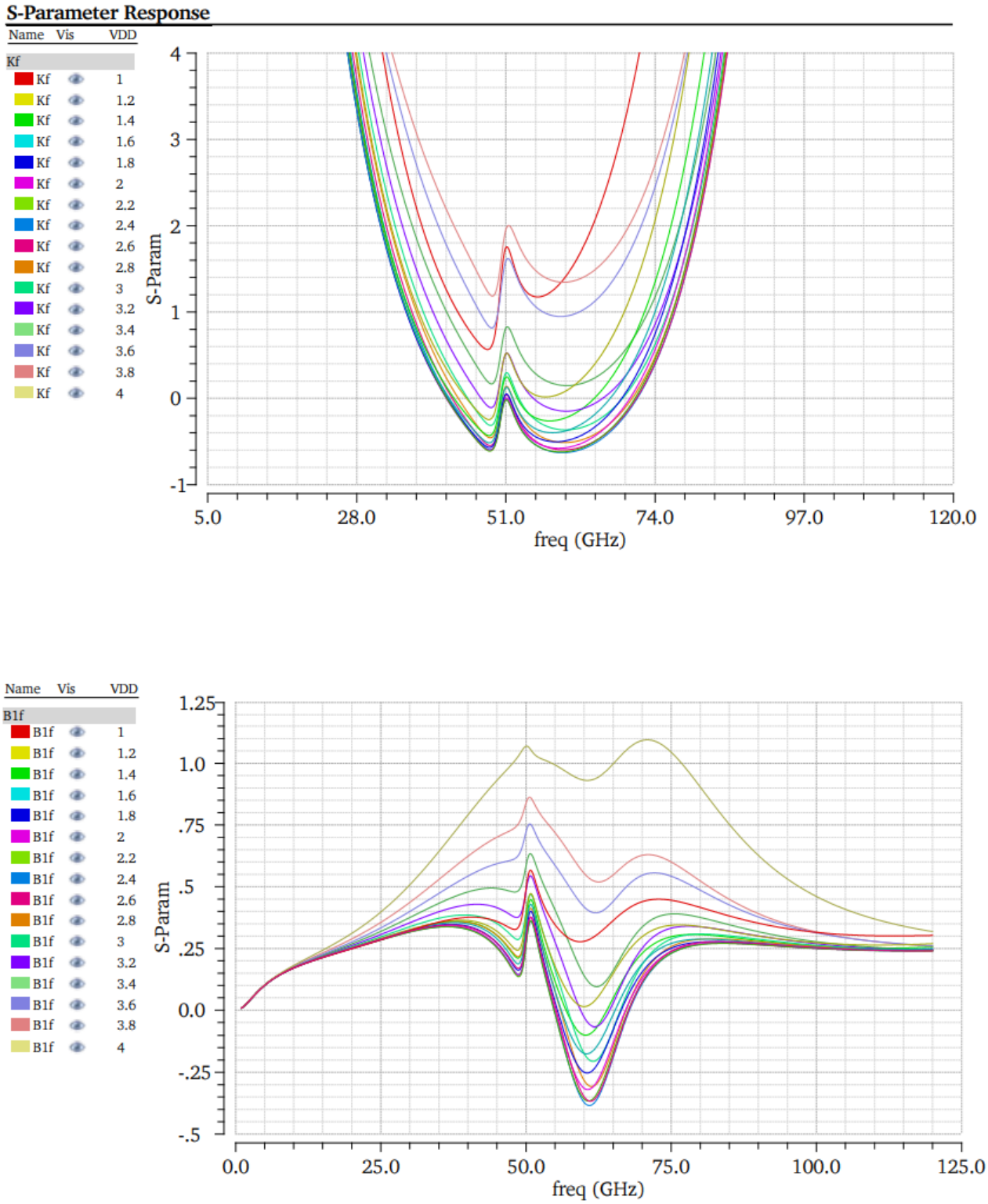

Figure 56 – K and B1 parameter analyses under different bias.

input and output, DC probe for the supply, and using the substrate of alumina beneath the chip. The first measurements with this setup were performed with the spectrum analyzer connected, but the signal generator disconnected (i.e., with the GSG input probe lifted). The results are presented in Table 6. Then we performed the same measurements with the signal generator connected, i.e., a source impedance of 50 Ω. The results of this last setup are presented in Table 7.

VDD (V)	Sample 5		Sample 6		Sample 7	
	IDD (mA)	Oscillations (dBm@GHz)	IDD (mA)	Oscillations (dBm@GHz)	IDD (mA)	Oscillations (dBm@GHz)
0.5	0.000015	No	0.00002	No	-	-
0.75	0.165	No	0.15	No	-	-
1	5.65	No	5.2	No	5.66	No
1.1	8.39	No	7.77	Yes -16@33.45	8.36	No
1.2	10.97	Yes -13.7@33.3	10.16	Yes -9.2@33.55	10.9	Yes -15@33.4
1.3	13.5	Yes -10.4@33.5	12.5	Yes -7@33.65	13.5	Yes -11.5@33.5
1.5	18.3	Yes -7.4@33.6	16.99	Yes -5@33.77	18.29	Yes -10@33.64
2.0	28.5	Yes -2.0@33.6	26.6	Yes -0.5@33.85	28.4	Yes -3.5@33.7
2.5	35.4	Yes 0.6@33.5	33.57	Yes 2.5@33.76	35.3	Yes -1.2@33.64
3.0	42.0	Yes 2.5 @33.6	40.2	Yes 3.5@33.87	42.0	Yes 0.9@33.7
3.5	49.3	Yes 0.73@33.84	47.6	Yes 2@34.15	49.64	Yes -2.3@34
4.0	58.1	Yes -4@33.15	55.16	Yes 4.5@34.41	-	-
4.5	67.7	Yes 5@34.6	-	-	-	-

Table 6 – Measurements with the PA input left open.

VDD (V)	Sample 8		Sample 9	
	IDD (mA)	Oscillations (dBm@GHz)	IDD (mA)	Oscillations (dBm@GHz)
1	5.78	No	5.33	No
1.5	18.79	Yes -18@29.56	17.16	No
2.0	29.92	Yes -7.8@29.56	27.35	Yes -54@30.64
2.5	39.88	Yes -2.92@30.64	36.46	Yes -6.86@30.64
3.0	48.85	Yes -3.45@31.84	45.11	Yes -3.5@32
3.2	51.46	Yes -9.15@31.84	47.95	Yes -4.7@32
3.3	52.62	Yes -40@31.3	49.17	Yes -7@332
3.4	53.8	No	50.17	Yes -13@32
3.5	54.97	No	51.15	No
3.6	56	No	52.2	No
3.7	57.26	No	53.14	No
3.8	died	died	54	No
3.9			died	died

Table 7 – Measurements with a 50 Ω connected to the input of the PA.

As can be seen from Tables 6 and 7 the circuit is unstable for most bias conditions in both cases (with the generator connected and disconnected). The DC behavior of the circuit can also be verified through the tables. It can be observed that the samples systematically burned close to 4 V, which probably indicates a thermal modeling problem of the transistors, since this bias condition keeps the transistor in an operating region below its theoretical limit in simulations. This burning of the circuit may be related to the thermal coupling between the three common-base transistors. Further research is needed to verify that the thermal impedance of the transistors was well modeled by the transistor model and to investigate the thermal coupling between the devices under different layouts. Unfortunately, no further information is contained in the technology manual, as "suggested values (for the thermal coefficients) as a function of the relative spacing between device layouts are planned for a future release" is mentioned in it (IBM, 2011). In the next chapter, the conclusions and prospects of this work will be discussed.

5 Conclusions and prospects

This master's thesis presented the design flow of a power amplifier in the 60 GHz band targeting future 5G applications. It was used a SiGe-based process from Global Foundries (BiCMOS8HP 0,13 μm). At the outset, a review of the literature on key fundamentals is done aiming at a good understanding of each step of the design flow. A review of the state of the art in SiGe PAs was also made to establish specifications, trends and to define good strategies of design to follow. A load-pull analysis was implemented including parameters to be optimized (bias and geometric parameters) in order to extract the best possible performance at 60 GHz from the transistors. For this the transistors are taken to operate in their limits of operation, in a weak avalanche region. A layout-oriented design approach (divided in four steps) was proposed to decide upon different combinations/arrangements of passive components and interconnections, aiming at reducing the losses of the amplifier, thus increasing its efficiency. The partitioning of the design allows each step of the layout to be refined (through several iterations) aiming at reducing parasitic elements, thus maximizing the performance in each step. This approach allowed us to get a very good relation between schematic and layout performances, by avoiding the huge discrepancies that may exist in the passage from the complete schematic circuit to the layout.

The post-layout results show a saturated output power of 19.32 dBm, a maximum PAE of 27.8 % with 10.4 dB of transducer gain and a 1 dB compression point (OP_{1dB}) of 19.1 dBm at 60 GHz. The amplifier is matched at the input and output with an almost flat gain greater than 10 dB across the entire unlicensed band (57 to 66 GHz). It consumes 63 mA of a 4.4 V power supply and occupies an area of approximately 0,475 mm^2.

This amplifier was part of a tape-out in late 2017 by MOSIS. The chips arrived in late May 2018 and measures took place in August of that year. The first experimental results showed that the circuit did not behave as expected. It was observed instabilities in bias conditions lower than nominal, indicating that the stability test not only must be performed under a very large frequency range, but also under different bias values. It was also observed that the samples of the circuit burned close to 4 V, indicating a possible problem in the thermal modeling of the transistors. One of the main limitations of this work that may explain the experimental results was the use of a RC-type extraction of the layout at such high frequencies, where electromagnetic simulations are more appropriate. Another possibility that should also be investigated is the use of transmission lines with ground-plane (the rfline line does not contain it). For future works on the design of 60 GHz power amplifiers some points are interesting to be investigated, they are:

1. Follow the same design flow of this work including electromagnetic simulations.
2. Perform stability analysis under a vast frequency range and under different bias conditions.
3. Perform large-signal stability analysis.
4. Investigate the thermal model of the transistors and verify the thermal coupling impact on temperature for different layouts interconnections of the same device, taking into account the following trade-off:
   - large spacing → larger layout parasites.
   - small spacing → higher thermal coupling.
5. Investigate the use of transmission-lines with and without ground-planes.
6. Investigate the design of power amplifiers with this methodology including power combining techniques, at the cost of higher power consumption and area.

This thesis was the subject of a scientific paper entitled "Layout-oriented Design of a 60 GHz Power Amplifier in SiGe", in the 33^{rd} South Symposium on Microelectronics (SIM 2018) presented in May 2018 in Curitiba, Paraná, Brazil (SETTE; SOUZA; DUPOUY, 2018).

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Appendix

Appendix A - Topologies performance Comparison

To ensure that the cascode topology is the best in terms of performance for the geometric parameters (table 4) obtained by optimization, the three topologies were compared here. For the common-base and cascode configuration, the VDD remains 4.4V and VB 1.8V. For the common-emitter configuration, the VDD was set at 2 V (slightly higher than BV_{ceo}). For each topology, load-pull simulations were performed for several bias current values. Through this it was possible to obtain the maximum value of Pout, PAE and gain as a function of the bias current (collector current). These simulations were performed using different input power levels (available from the source): 5, 7.5 and 10 dBm. The results are shown in the figures below. It can be observed that for the three cases of input power, the cascode configuration exhibits Pout, PAE and gain (simultaneously) results within our specifications with a bias current close to 60 mA. It is also important not to use a high bias current, thus reducing the power consumption of the amplifier.

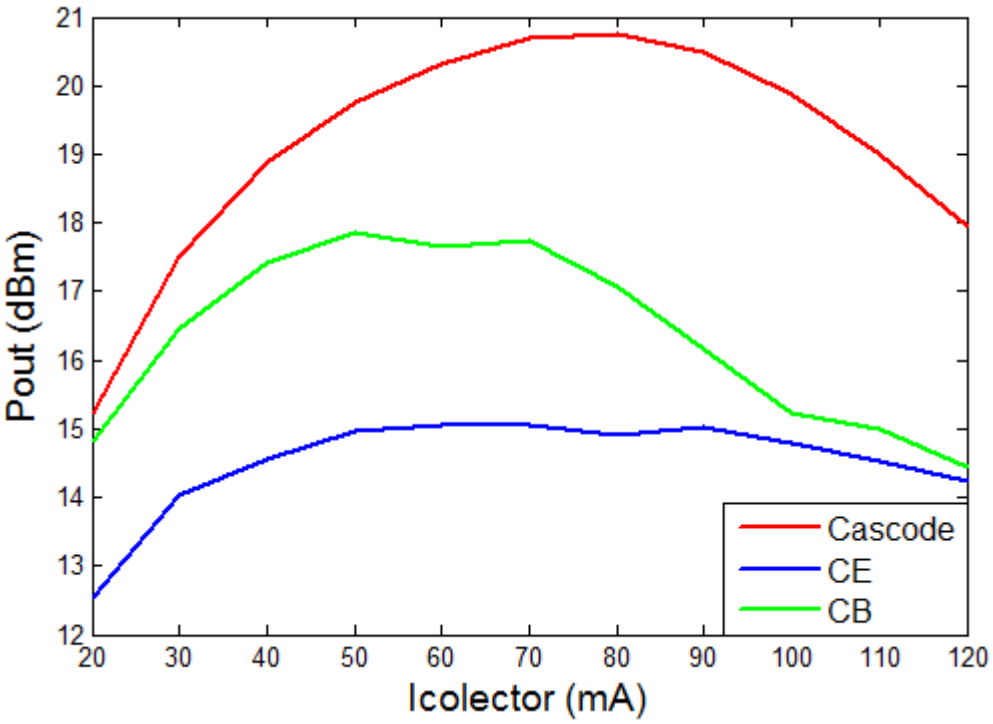

Figure 57 – Pout with 5 dBm of Pavs.

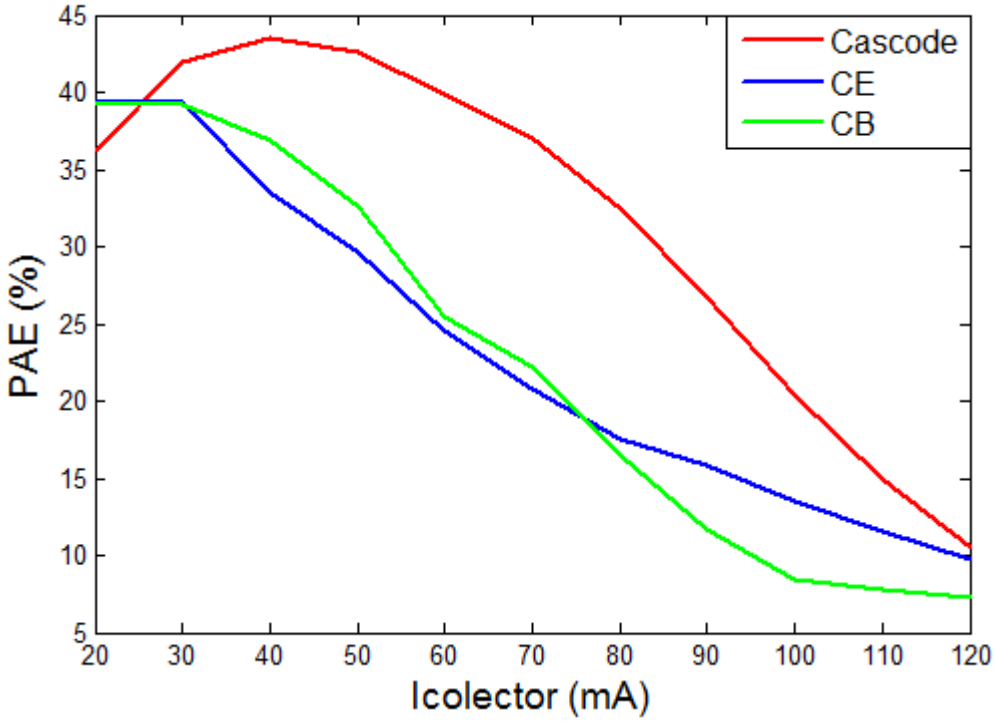

Figure 58 – PAE with 5 dBm of Pavs.

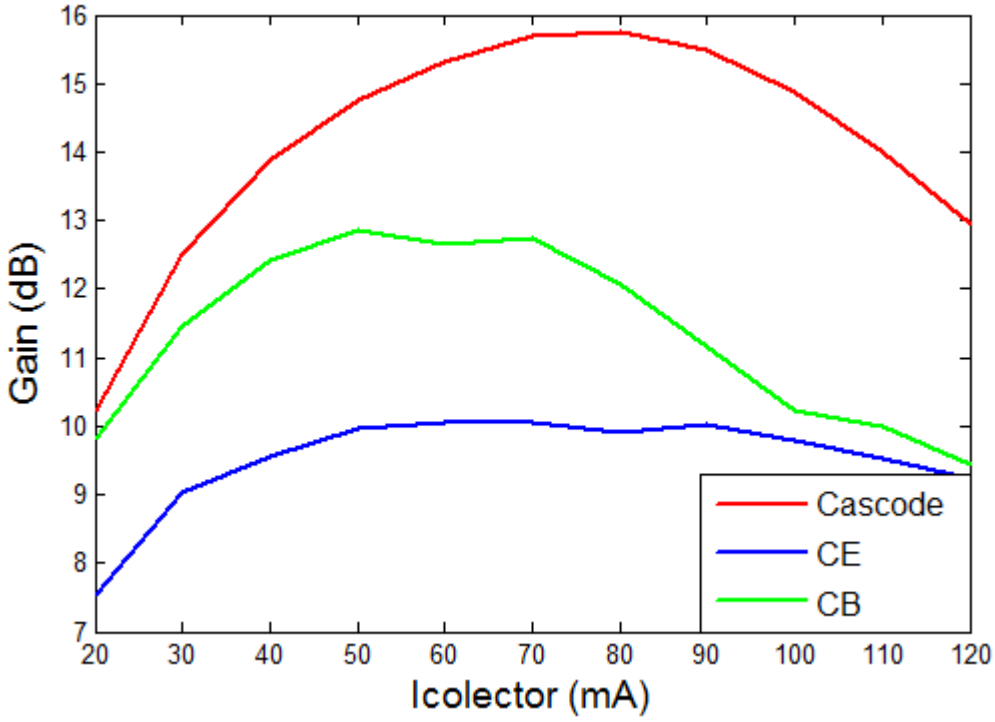

Figure 59 – Gain with 5 dBm of Pavs.

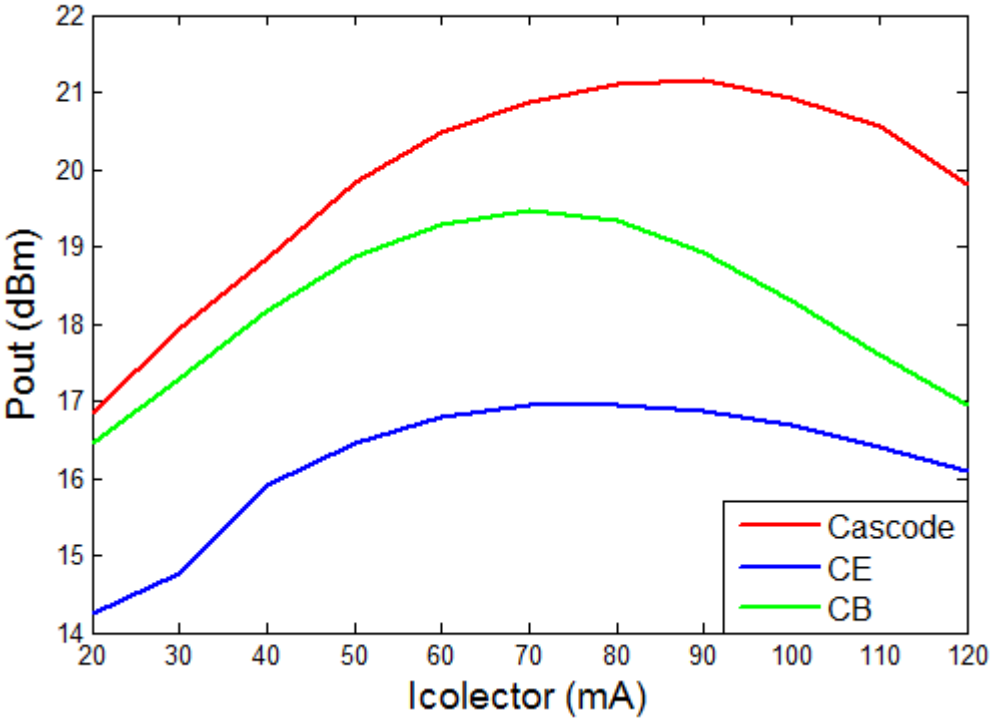

Figure 60 – Pout with 7.5 dBm of Pavs.

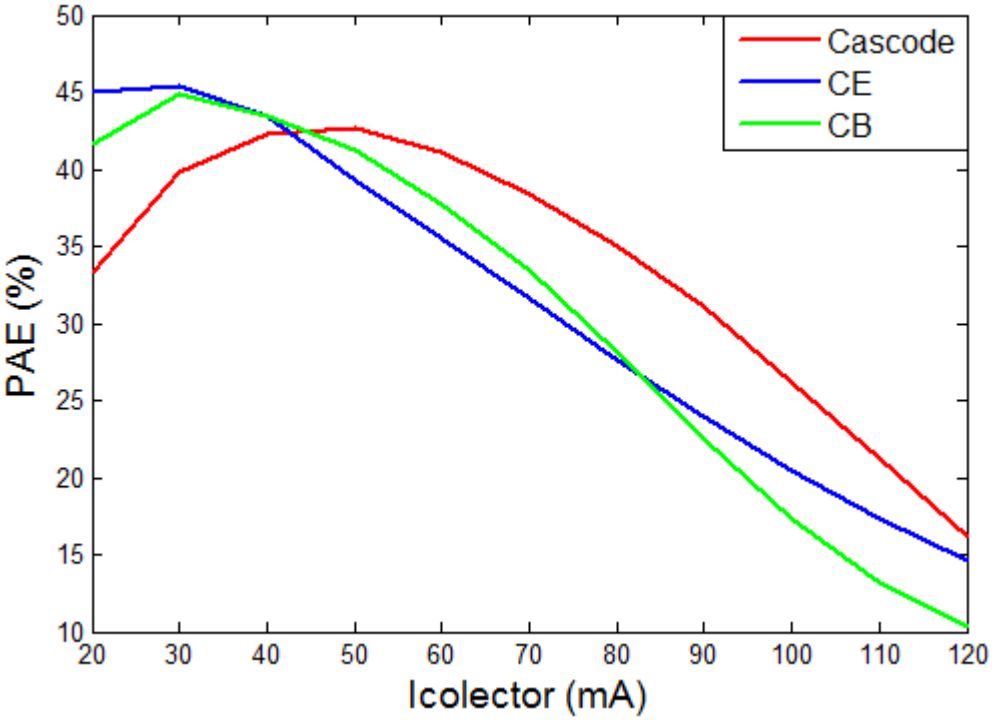

Figure 61 – PAE with 7.5 dBm of Pavs.

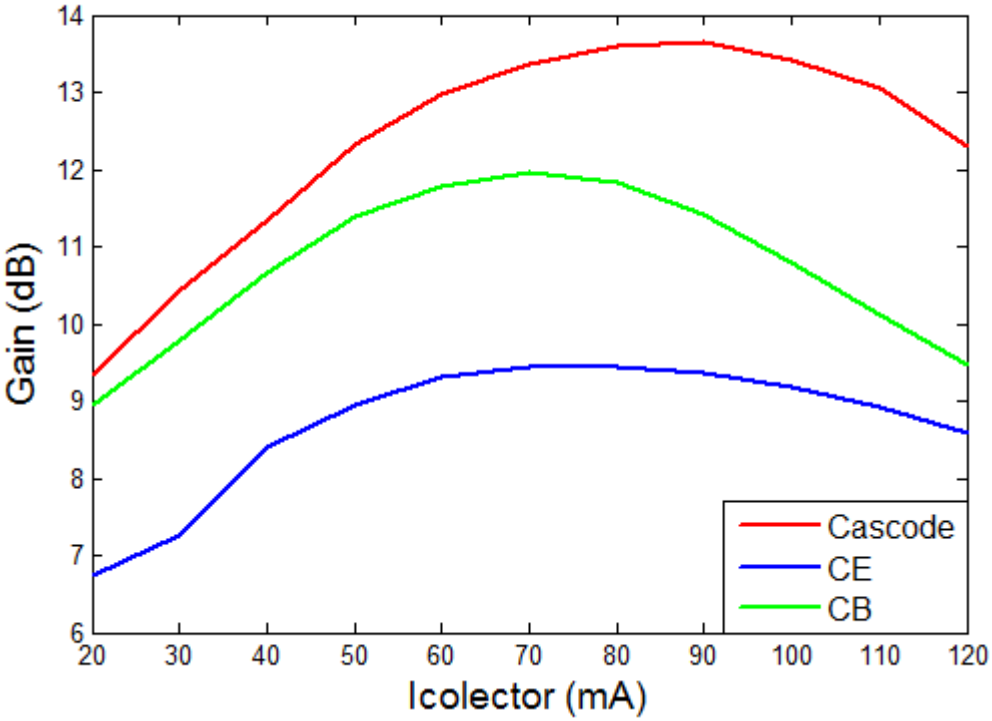

Figure 62 – Gain with 7.5 dBm of Pavs.

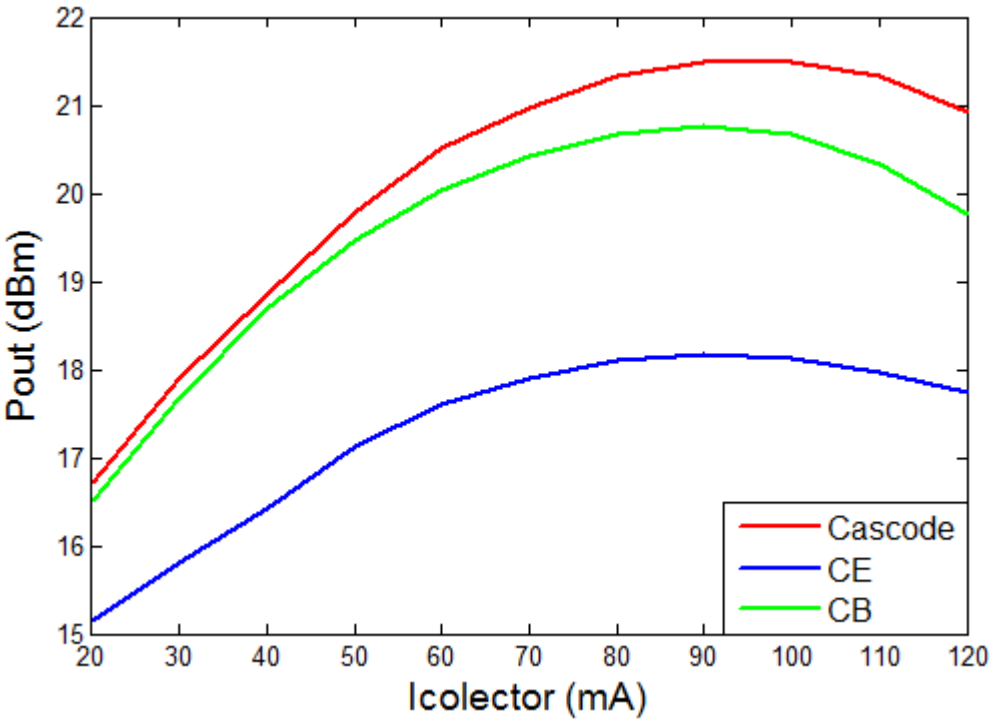

Figure 63 – Pout with 10 dBm of Pavs.

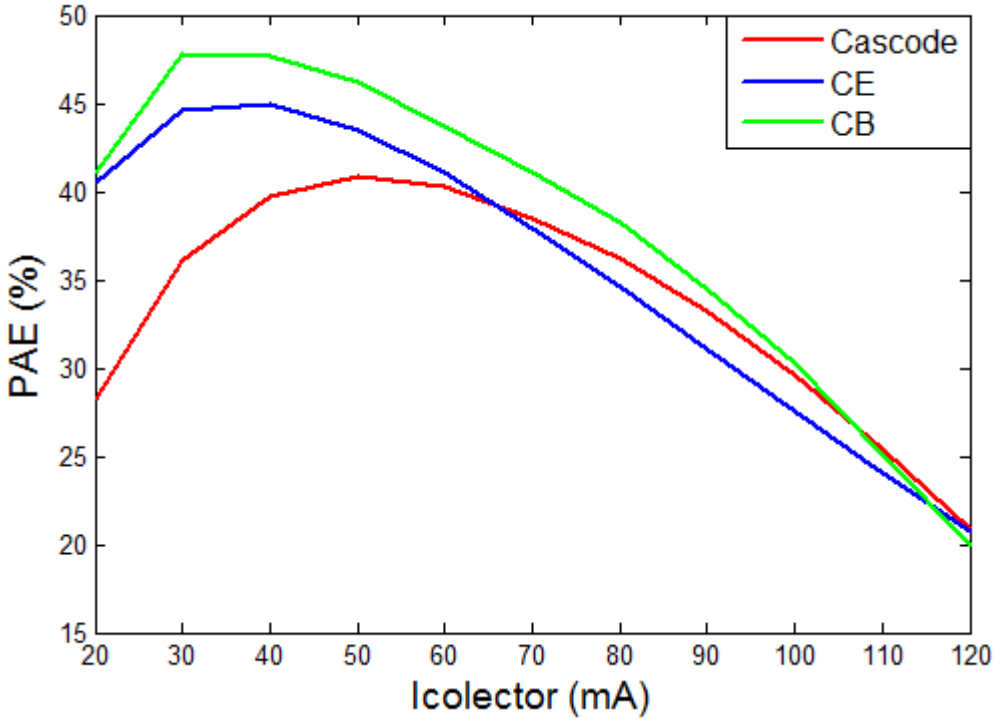

Figure 64 – PAE with 10 dBm of Pavs.

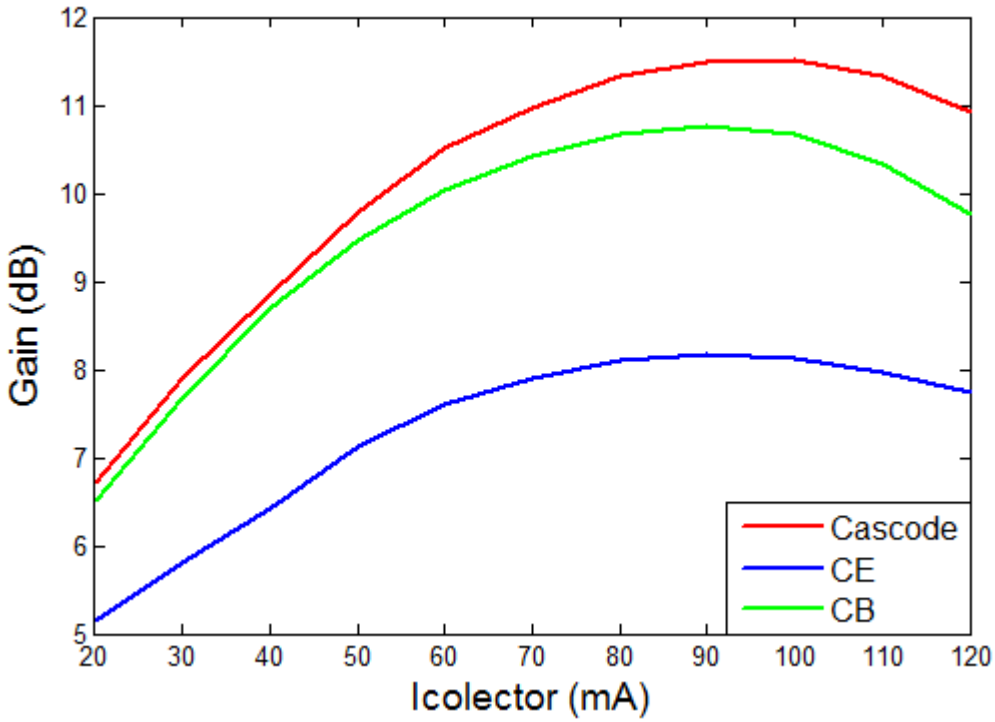

Figure 65 – Gain with 10 dBm of Pavs.